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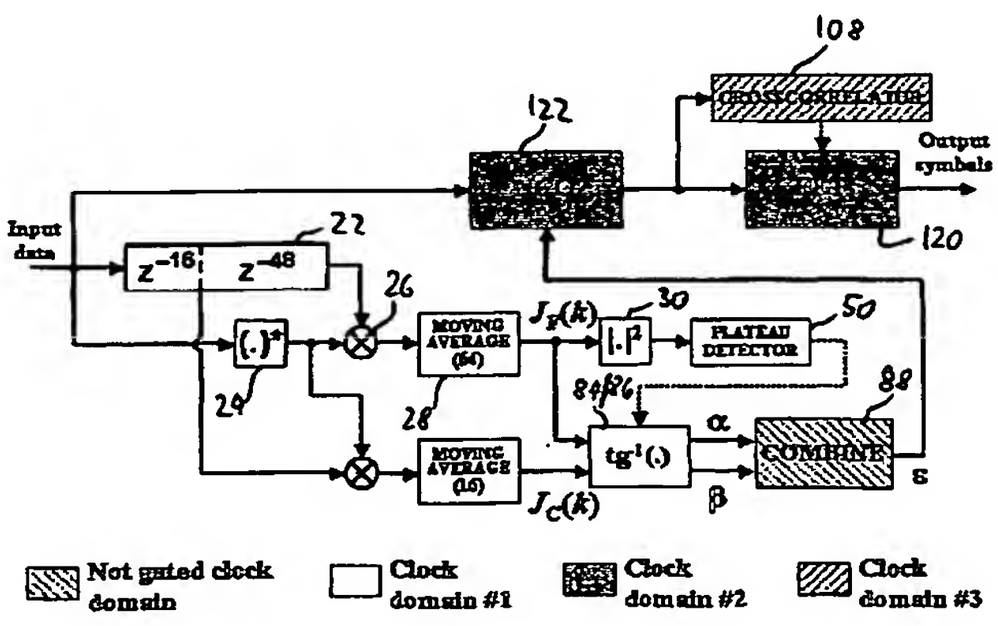

(57) Abstract: The IEEE 802.11 a standard makes use of the Orthogonal Frequency Division Multiplex (OFDM) transmission scheme. The main feature of the OFDM is that the information stream is not transmitted into a single carrier, but is divided into several sub-carriers, each transmitting at a much lower rate. Furthermore, all these sub-carriers are orthogonal, i.e. they overlap their spectra but without causing mutual interference. In summary, there are the following inventions comprised in present application: the algorithm used for the frame detection, making use of a simplified differentiator to obtain an absolute maximum in the differentiated signal at that point where the first plateau in $J_F(k)$ starts (output of the autocorrelator with N_d=64); the design of the peak detector to obtain the position of the absolute maximum in the differentiated signal, dividing the problem into relative peak detection and falling edge detection; the use of a simplified XNOR-based crosscorrelator, and the simplifications therein based on the knowledge of the reference; the use of our particular solution for the CORDIC algorithm in the vectoring mode for arctangent calculation; the hardware structuring of the whole synchronizer, allowing a very simple control mechanism and the separation of this structure into different clock domains, each one being activated only to perform its operation and deactivated afterwards.

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Method and Device for Frame Detection and Synchronizer

The present invention concerns a method for the detection of the reception of a data frame in an input signal, said data frame comprising periodically repeated symbols at the beginning. It further concerns a frame detector, a synchronizing method, and a synchronizer device.

BACKGROUND OF THE INVENTION

The IEEE 802.11a standard makes use of the Orthogonal Frequency Division Multiplex (OFDM) transmission scheme. The main feature of the OFDM scheme is that the information stream is not transmitted into a single carrier, but is divided into several sub-carriers, each transmitting at a much lower rate.

Furthermore, all these sub-carriers are orthogonal, i.e., they overlap their spectra, but do not cause mutual interference.

The fact that the different sub-carriers overlap their spectra makes one of the main operations at the receiver especially difficult: synchronization. In a receiver, the synchronizer is the block responsible for detecting the incoming frame and for estimating and correcting possible frequency offsets. The synchronization process is also responsible for providing a reference channel estimation to the channel estimation block. It further decides the starting point from which on the different OFDM symbols will be fed into the FFT block. The correct reception of OFDM signals is very sensitive to the synchronizer performance.

In the OFDM transmissions considered here, the information is not transmitted continuously, but in bursts. Each burst contains a single frame, which is a compound of different OFDM symbols.

In an OFDM transmission each data packet consists of a preamble and a data carrying part. The preamble symbols are placed at the very beginning of each frame during transmission. The preamble consists of 10 "short" identical known OFDM symbols concatenated with 2 "long" identical and known OFDM symbols. The preamble symbols have a very specific periodic structure in the standard IEEE 802.11a to simplify synchronization. The data carrying part consists of a variable number of OFDM symbols, where each OFDM symbol contains useful information plus some known pilot sub-carriers, which are typically used for phase tracking.

Synchronization comprises the following operations: Frame detection, carrier frequency offset determination, symbol timing estimation, extraction of the reference channel, and data reordering. The synchronization process is data-aided, i.e., based on the digital processing of the preamble symbols.

During reception, the synchronizer has to peer the channel in order to detect an incoming packet or frame. Frame detection in a receiver is an especially difficult task because there is no time raster that governs the transmission of

the frames. In other words, the receiver does not know when to expect an incoming frame. The object of frame detection is to determine the symbol boundary so that correct samples for a frame can be taken. A major problem in the use of OFDM is therefore the determination of the time instant, at which the receiver starts sampling a new frame. A mismatch in the determination of this parameter would introduce a phase error causing intercarrier interference (ICI).

A method for frame detection in an OFDM signal is described by Chiu et al. (Yun, Chiu, Dejan Markovic, Haiyun Tang, Ning Zhang, OFDM receiver Design, published at URL: http://bwrc.eecs.berkeley.edu/People/Grad_Students/dejan/ee225c/ofdm.pdf). It uses the first ten short symbols transmitted at the beginning of an OFDM frame, also referred to as the "short traning sequence". The waveform of the short symbols is known and stored in the receiver decive. The receiver performs a correlation of the sampled signal with the stored waveform. It further performs and autocorrelation of the sampled signal with the delay of one short symbol. While the autocorrelation creates a first signal with a plateau over a time span during which short symbols are received, the correlation with the known waveform creates a second signal exhibiting peaks. The last peak of the second signal occurring during a plateau in the first signal is chosen as a time reference to start frame detection.

However, in the solution proposed by Chiu et al. the frame detection does not work if a fading channel is affecting the signal.

Another method is described in Schwoerer, L.; Wirz, H.; "VLSI Implementation of IEEE 802.11a Physical Layer". Proceedings of the 6th International OFDM-Workshop (InOWo) 2001, pp. 28.1-28.4, Sept. 2001, Hamburg, Germany. To detect the periodicity of the short training sequence, a sum of the absolute amount of three delayed autocorrelation terms over three different, overlapping time spans is calculated and then compared to a threshold value that is scaled with the signal power over the same time spans.

The solution proposed by Schwoerer et al. correspondingly makes use of three autocorrelators for the frame detection. This implies a rather large silicon area necessary for implementation of their solution and a high power consumption.

Summary of the Invention

It is an object of the invention to provide a simple and reliable method and device for detection of the reception of a data frame in an input signal.

It is a further object of the invention to provide a synchronizing method and a synchronizer with a simple and reliable frame detector.

These objects are solved with a frame detection method according to claim 1, a frame detector according to claim 14, a synchronizing method according to claim 17, and a synchronizer device according to claim 26.

According to a first aspect the invention a method for detection of the reception of a data frame in an input signal (y_{OFF} (n)) is provided. The method is based on the fact that the data frame comprises periodically repeated symbols at the beginning. The method of the first aspect of the invention comprises the steps of

a) sampling said input signal (y_{OFF} (n)) with a predetermined sampling rate

b) generating a first signal ($|J(k)|^2$) that is dependent on an autocorrelation of said input signal with a delayed copy of said input signal, and

c) detecting a plateau in said first signal ($|J(k)|^2$)

d) generating an output signal that is indicative of detecting said plateau.

In the method of first aspect of the invention, step c), i.e., detecting a plateau, comprises a step of generating a differentiator signal (J_{diff} (k)), which is dependent on the difference of a first sample of the first signal and a second sample of the first signal that was taken a predetermined number of sampling periods earlier. Further, step c) comprises a step of detecting an absolute maximum of said differentiator signal (J_{diff} (k)) within a predetermined range of sampling periods.

The method of the invention makes use of the fact that a plateau in an autocorrelation signal, i.e., in the first signal, can be detected reliably by making use of a differentiation of the autocorrelation signal with a limited bandwidth. As is known, a plateau in the autocorrelation signal is indicative of the reception of a frame with periodically repeated symbols in the input signal.

The invention is based on the finding that a real differentiation, that is, a differentiation with a limited bandwidth, will transform an input signal into an output signal that exhibits an absolute maximum at the onset of a plateau of the input signal. In the method of the invention, the input to the real differentiation is the autocorrelation signal, and the output signal is the differentiator signal. The bandwidth of the differentiation can be limited for instance by calculating the difference of the respective two autocorrelation signals involved with a predetermined delay of a number of sampling periods.

A maximum of the differentiator signal can be detected with precise timing in a simple and reliable manner with an appropriate peak detection method.

An ideal differentiator, that is, a differentiator with an unlimited bandwidth, would show a discontinuity at the onset of a plateau, assuming that no noise was present in the signal.

It is noted that the term signal as used herein denotes, depending on the context, analog signals or digital signal, for instance binary representations of values of quantities, such as for instance a digital representation of a number indicating the current value of an autocorrelation of the input signal with its delayed copy.

The step of generating said differentiator signal (J_{diff} (k)) comprises for instance a step of delaying the first signal ($|J(k)|^2$) for the first predetermined number of sampling periods, and a step of generating a difference signal that is dependent on the difference between the first signal ($|J(k)|^2$) of a current sampling period and the delayed first signal ($|J(k)|^2$).

In a preferred embodiment of the invention, the autocorrelation step (step b) comprises the steps of delaying the input signal by a third predetermined number (N_d) of sampling periods, transforming the input signal into a second signal that is dependent on the complex conjugate of the input signal, and generating a fourth signal that is dependent on the product of said second signal and of said delayed input signal. Preferably, an autocorrelation signal is generated that is dependent on a sum of a fourth predetermined number N_{avg} of autocorrelation signals.

To accomplish the calculation of the sum, a fourth signal can be saved for N_{avg} sampling periods. The autocorrelation signal is created by adding said fourth signal of a current sampling period to said autocorrelation signal of a last previous sampling period and subtracting one fourth signal, that was saved N_{avg} sampling periods earlier. Preferably then, the first signal is obtained as the product of the autocorrelation signal and its complex conjugate.

In a further preferred embodiment, the step of detecting an absolute maximum of the differentiator signal within a second predetermined number of sampling periods comprises an instantaneous peak detection step and a step of detecting a falling slope in the differentiator signal. Preferably, these two steps are performed in parallel. Instantaneous peak detection refers to the detection of a relative peak in the differentiator signal. The detection of a relative peak at the same time a falling slope occurs is an indication of the occurrence of an absolute maximum in the signal within the second predetermined number of sampling periods. In this embodiment, the detection of an absolute maximum in the differentiator signal is implemented with a simple and reliable method.

Instantaneous peak detection involves, for instance, comparing the differentiator signal (J_{diff} (k)) of a current sampling period with the differentiator signal (J_{diff} (k)) of a last, i.e., a next previous sampling period, and a step of saving the differentiator signal (J_{diff} (k)) of the current sampling period to a register, given the condition that its value is larger than that of the differentiator signal (J_{diff} (k)) of the previous sampling period. The register therefore always contains the largest differentiator signal.

Preferably, a step of incrementing a count index by one is performed, if the value of said differentiator signal (J_{diff} (k)) of the current sampling period is equal or smaller than that of said differentiator signal (J_{diff} (k)) saved in said register. A (third) signal can be generated indicative of the condition whether or not the count index has reached a predetermined value. The third signal indicates that a relative peak has been found within the sample range defined by the predetermined counter value, which can be the counter limit. The relative maximum is the value contained in the register.

Detection of a falling slope in the differentiator signal (J_{diff} (k)) is preferably performed by a group peak detection method. That means, the differentiator signal is accumulatord in groups of six samples and the present group is compared with the previous one. If the present group is smaller than the previous one, the falling slope has started. In detail, an accumulation signal is generated that is dependent on the sum of the differentiator signal (J_{diff} (k)) over a predetermined accumulation number of consecutive sampling periods. The current accumulation signal is compared with the last previous accumulation signal representing (without overlap) the accumulation number of consecutive earlier sampling periods. If the value of the current accumulation signal is smaller than the value of the earlier accumulation signal, a group peak detection signal is generated. In an alternative embodiment, the group peak detection is a binary signal that is for instance "0" if the current accumulation signal is larger, and "1" if the current accumulation signal is smaller than the previous one. The group peak detection signal thus indicates that the differentiator signal is decreasing.

A maximum detection signal can be generated if the instantaneous peak detection signal indicates that the count index has reached the predetermined count value and the group peak detection signal indicates that the value of the current accumulation signal is smaller than the value of the earlier accumulation signal. Preferably, the maximum detection signal is the output signal.

It is noted that with the peak detection algorithm described above the plateau will be detected with a small delay due to the instantaneous peak detection method. The delay corresponds to the predetermined count value used in the instantaneous peak detection. However, this delay has no influence on the result of the following steps in the synchronization.

Preferably, the input signal is amplified such that the power of the amplified input signal is in a predetermined power range. The purpose of this step is to adapt the input power to a power level according to the conversion range of Analog-Digital converters. In order to avoid detecting a plateau in pure noise, the step of detecting a plateau in the first signal ($|J(k)|^2$) is preferably performed only if the first signal $|J(k)|^2$ exceeds a predetermined threshold value.

The method of the invention is preferably used for detecting a data frame containing OFDM symbols.

According to a second aspect of the invention, a frame detector is provided for detecting the reception of a data frame in an input signal (y_{OFF} (n)), said data frame comprising periodically repeated symbols at the beginning. The frame detector has

a) a sampling unit adapted to sample said input signal (y_{OFF} (n)) with a predetermined sampling rate

b) an autocorrelation unit adapted to transform said input signal (y_{OFF} (n)) into a first signal ($|J(k)|^2$) that is dependent on an autocorrelation of said input signal with a delayed copy of said input signal, and

c) a plateau detector, adapted to detect a plateau in said first signal ($|J(k)|^2$)

d) an output unit adapted to generate an output signal that is indicative of detecting said plateau.

The plateau detector is adapted to generate a differentiator signal (J_{diff} (k)), which is dependent on the difference of a first sample of said first signal and a second sample of said first signal a predetermined number of sampling periods earlier, to detect an absolute maximum of said differentiator signal (J_{diff} (k)) within a predetermined range of sampling periods, and to provide a signal indicative of detecting said absolute maximum to said output unit.

The frame detector of the second aspect of the invention implements the frame detection method of the first aspect of the invention. In what regards advantages reference is made to the above description of the method of the invention.

A preferred embodiment of the frame detector of the second aspect of the invention implements the plateau detection method according to the preferred embodiment of the method of the invention described earlier. Preferably, said plateau detector of the frame detector comprises a peak detection unit with a first detection unit connected to the input port and comprising a first memory unit. The first detection unit is adapted to compare the input signal (Jdiff (k)) received through the input port with a first entry contained in the first memory unit, and to replace the first entry by the input signal if the value of the input signal (Jdiff (k)) is larger than the value of the first entry. The first detection unit implements the instantaneous peak detection method.

In this embodiment, there is preferably a second detection unit connected to the input port and comprising a second memory unit. The second detection is adapted to generate an accumulation signal that is dependent on the sum of the differentiator signal (J_{diff}(k)) over a fourth predetermined number of consecutive sampling periods, to compare the current accumulation signal

with the last previous accumulation signal representing without overlap the fourth predetermined number of consecutive earlier sampling periods, and to generate a group peak detection signal indicative of whether or not the value of the current accumulation signal is smaller than the value of the earlier accumulation signal.

Further preferred embodiments of the frame detector implement preferred embodiments of the frame detection method described earlier. From that description it is obvious to a person skilled in the art how to implement the preferred embodiments of the frame detector.

It is noted that the peak detection method as well as the peak detection unit used in the present context for detecting a plateau in the autocorrelation signal can be used for peak detection in any signal. The peak detection method as well as the peak detection unit represent an independent invention.

According to a third aspect of the invention, a synchronizing method is provided. The synchronizing method comprises a step of frame detection, which is carried out using the method of the first aspect of the invention or any of its embodiments described above or in the dependent claims.

A carrier frequency offset, which is due to a frequency mismatch during RF downconversion, introduces an unknown phase factor to each signal sample. This unknown phase factor must be estimated and compensated for each sample before performing a Fast Fourier Transform (FFT) at the receiver. Otherwise the orthogonality between subcarriers is lost. A loss of orthogonality is also creates intercarrier interference.

A preferred embodiment of the synchronizing method of the third aspect of the invention therefore further comprises a step of estimating a relative frequency offset (f_ε) in an input signal ($y_{OFF}(n)$), wherein the estimating step comprises the steps of

a) estimating a coarse frequency offset (β)

b) estimating a fine frequency offset (α) in dependence of said estimated coarse frequency offset (β).

In this embodiment, the steps of estimating a coarse frequency offset (β) and/or of estimating a fine frequency offset, i.e., step a) or b) or both steps a) and b), preferably comprise a step of calculating a phase value of said first signal ($|J(k)|^2$).

The step of estimating the frequency offset comprises in one embodiment a step of assigning a fine frequency offset value dependent on the value of the coarse frequency offset according to the following function:

$\varepsilon=\alpha$; if $(-0.1)/4 \leq \beta \leq (0.1)/4$ (R1)

$\varepsilon=\alpha$; if $\alpha \geq 0$ and $(0.1)/4 < \beta < (0.9)/4$ (R2)

$\varepsilon=1+\alpha$; if $\alpha < 0$ and $(0.1)/4 < \beta < (0.9)/4$ (R3)

$\varepsilon=1+\alpha$; if $\beta \geq (0.9)/4$ (R4)

$\varepsilon=-1+\alpha$; if $\alpha \geq 0$ and $(-0.9)/4 < \beta < (-0.1)/4$ (R5)

$\varepsilon=\alpha$; if $\alpha < 0$ and $(-0.9)/4 < \beta < (-0.1)/4$ (R6)

$\varepsilon=-1+\alpha$; if $\beta \leq (-0.9)/4$ (R7)

In an alternative embodiment that is slightly more robust to noise than the embodiment just described the step of assigning a fine frequency offset value dependent on the value of the coarse frequency offset is performed according to the following function:

$\varepsilon=\alpha$; if $(-0.25)/4 \leq \beta \leq (0.25)/4$ (R1)

$\varepsilon=\alpha$; if $\alpha \geq 0$ and $(0.25)/4 < \beta < (0.75)/4$ (R2)

$\varepsilon=1+\alpha$; if $\alpha < 0$ and $(0.25)/4 < \beta < (0.75)/4$ (R3)

$$\varepsilon=1+\alpha \quad ; \text{if } \beta \geq (0.75)/4 \tag{R4}$$

$$\varepsilon=-1+\alpha \quad ; \text{if } \alpha \geq 0 \text{ and } (-0.75)/4 < \beta < (-0.25)/4 \tag{R5}$$

$$\varepsilon=\alpha \quad ; \text{if } \alpha < 0 \text{ and } (-0.75)/4 < \beta < (-0.25)/4 \tag{R6}$$

$$\varepsilon=-1+\alpha \quad ; \text{if } \beta \leq (-0.75)/4 \tag{R7}$$

Preferably, after estimation the frequency offset, a step of correcting the input signal by the estimated value is performed.

A further embodiment of the synchronizing method of the invention comprises after said step of frequency offset correction a step of estimating the time of reception of at least one symbol contained in a received data frame (hereinafter referred to as a symbol timing step).

The symbol timing step preferably comprises a step of generating a crosscorrelation signal, which is dependent on the value of the crosscorrelation of the corrected input signal with a known reference signal, wherein the reference signal is a first section of long preamble symbols included in the data frame. In a preferred embodiment, the reference signal is 32 samples long.

Another embodiment comprises a step of estimating a reference channel, preferably using a step of performing a Fast Fourier Transform of a second section of the long preamble symbols included in the data frame.

According to a fourth aspect of the invention, a synchronizer device is provided. The synchronizer device comprises a frame detector according to an embodiment of the frame detector of the second aspect of the invention.

The synchronizer device preferably further comprises a symbol timing unit adapted to generate a crosscorrelation signal, which is dependent on the value of the crosscorrelation of the corrected input signal with a known

reference signal, wherein the reference signal is a first section of long preamble symbols included in the OFDM frame.

The symbol timing unit comprises in one embodiment a crosscorrelation unit with a number of multipliers for complex numbers, and wherein at least one multiplier is made of a combination of XNOR-gates, inverter gates and adders.

To save power, the frame detection unit and the symbol timing unit can in one embodiment be enabled or disabled individually. This is preferably implemented by means to enable or disable the clock for the individual unit. It is noted that one clock is used for both units.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following, a preferred embodiment of a synchronizer device according to the invention will be described with reference to the figures.

Figure 1 shows the preamble symbols used in the IEEE 802.11a standard.

Figure 2 shows a scheme of a general delayed autocorrelator.

Figure 3 shows a detailed scheme of a moving average block in the autocorrelator of Fig. 2.

Figure 4 shows a signal at the output of the delayed autocorrelator for two possible values for N_d keeping $N_{avg} = N_d$.

Figure 5 shows a structure of an embodiment of a plateau detector,

Figure 6 shows a sketch of the signal $J_{diff}(k)$ at the output of the differentiator,

Figure 7 shows a detailed scheme of the several signals involved in the peak detection procedure.

Figure 8 shows a particular implementation of the peak detector.

Figure 9 shows the dependency of the phase of $J^*(k)$ with respect to the input carrier frequency offset (normalized) for two particular values of N_d

Figure 10 shows a scheme of a frequency offset estimator used in the synchronizer device.

Figure 11 shows the different decision regions for the combination of α and β in the frequency offset estimation and correction.

Figure 12 shows a timing diagram of the whole synchronization procedure.

Figure 13 shows a scheme of an XNOR-based complex multiplier.

Figure 14 shows possible simplifications of the XNOR-based complex multiplier if the input B is known a priori.

Figure 15 shows a structure of the crosscorrelator used for timing estimation.

Figure 16 shows the square magnitude of the output of the crosscorrelator when the reference signal is the portion of the long preamble symbols shown in Figure 12.

Figure 17 shows a general synchronizer scheme with different clock domains. Each clock domain is activated when it has to carry out some kind of operation. If not, it is disabled in order to reduce the power consumption of the whole synchronizer.

Figure 18 shows a representation of the two operation modes of the circular CORDIC algorithm being used in the synchronizer.

DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1 shows the structure of a preamble 10 of a frame used in the IEEE 802.11a standard. It is composed of ten short preamble symbols referred to as t_1, ..., t_{10}, each having a length of 0.8 µs. A short preamble symbol is sampled 16 times. Furthermore, there are two long preamble symbols 12 and 14 (ABCD-ABCD) with a double cyclic prefix 16 (CD), thus resulting in the structure CD-ABCD-ABCD of the second section of the preamble. The full preamble as shown has a duration of 16 µs. 8µs is the duration of the short ten preamble symbols, and 8 µs is the duration of the long preamble symbols with the cyclic prefix.

In the following, an embodiment of a frame detector is described in detail. The description also gives a clear picture of an embodiment of a method for frame detection that is implemented in the frame detector.

During synchronization the reception of a frame is to be detected. This detection is based on the particular periodic structure of the preamble symbols. The circuit used for this purpose is sketched in Figure 2, representing a scheme of a general delayed autocorrelator 20. It is based on an autocorrelation of the input signal with a delayed version of itself.

The autocorrelator has a delay block 22 introducing a delay of N_d clock cycles to an input signal $y_{OFF}(n)$. In parallel to delay block 22 a conjugator block 24 is provided that generates a complex conjugate of the input signal $y_{OFF}(n)$. The output signals of the delay block 22 and of the conjugator block 24 represent the input signals to a multiplication stage 26. The output of multiplication stage 26 is fed into a moving average block 28 that will be explained in further detail with reference to Fig. 3. The moving average of the input signal of block 28 consists of the addition of the most recent N_{avg} samples. The output signal $J(k)$ of moving average block 28 is fed into a block 30 that provides at its output the absolute amount of its input signal.

The output of the autocorrelation block can be expressed as

$$J(k) = \sum_{l=0}^{N_{avg}-1} y^*_{OFF}(l-k) \cdot y_{OFF}(l-k-N_d) \quad (1)$$

Two parameters are important here: N_d and N_{avg}. The former (N_d) is the length of the delay introduced by delay block 22 and the latter (N_{avg}) is the length of the *moving average* block.

The selected value for N_d directly depends on the periodicity found in the preamble. From Figure 1, several periodicities are possible, i.e. 16, 32, 48, 64 and 80 samples. Generally, the value for N_{avg} is selected to be the same as N_d.

Fig. 3 shows a detailed scheme of the moving average block 28 in the autocorrelator. Its structure is like that of in a Finite Impulse Response (FIR) filter, but with the advantage that all the coefficients are one. Thus, it is not necessary to add all the N_{avg} samples stored inside the register each time when a new sample comes in, but only add the new sample and subtract the oldest one.

The structure of the moving average block sketched in Figure 3 comprises N_{avg} delay elements, three of which are shown with reference signs 32, 34, and 36. Each delay element introduces a delay of one clock cycle. Delay element 32 is the first delay element in the signal flow, delay element 34 the second, and delay element 36 the last. Each of the delay elements works with a complex sample. The output of the last delay element 36 in the signal flow is fed as the subtrahend into a subtractor 38. Subtractor 38 receives a second input from an adder 40. Adder 40 adds the current content of a register 42 and the output of the first delay element 32. Register 42 contains the last output of subtractor 38.

Fig. 4 shows a signal at the output of the delayed autocorrelator 20 for two possible values for N_d, keeping $N_{avg} = N_d$. In Figure 4, the signal $|J(k)|^2$ is represented as a function of sample index, i.e. as a function of time, for N_d=16 (Fig. 4(A)) and N_d=64 (Fig. 4(B)). The output $J(k)$ is complex, and so the

square magnitude $|J(k)|^2$ is represented. It can be observed that $|J(k)|^2$ shows a region with a constant value (*plateau*) for a number of samples. In both cases N_d=16 and N_d=64, several regions showing a plateau are found. The length and position of the plateau directly depends on N_d. The plateau is longer and occurs earlier for N_d=16.

For reasons that we will clarify in the next section, when explaining the carrier frequency offset estimation, the embodiment described here uses N_d=64 and $N_{avg}=N_d$. The procedure to detect the frame is based on a plateau detection algorithm for the signal $|J(k)|^2$ (see Figure 4 (B)).

Figure 5 shows a structure of an embodiment of a plateau detector 50. The plateau detector 50 is separated into a *differentiator* block 52 and a *peak detector* block 54. Making use of a differentiator, the plateau detector 50 implements an algorithm that tries to find out the point where the first plateau starts. This is done according to the following principle: At the onset of a plateau, the function $|J(k)|^2$ is not differentiable and an ideal differentiator would show a discontinuity. A real differentiator has a limited bandwidth and so the discontinuity may not happen. In addition, as we are interested in a noise-robust system, this bandwidth has to be as small as possible. As the plateau is 32 samples long, we decided to use the differentiator shown in Figure 5 for the present embodiment, which is based on a delay line 56 of length 32 together with a subtractor 58.

The peak detection block 54 is divided into two sub-blocks: *group peak detector* 58 and *instantaneous peak detector* 60. The structure of the peak detector block 54 will be explained in detail below with reference to Fig. 8.

Figure 6 shows a sketch of the signal $J_{diff}(k)$ at the output of the differentiator block 52, when the input $|J(k)|^2$ is as in Figure 4 (B) with N_d=64. Both signals $J_{diff}(k)$ and $|J(k)|^2$ are shown in Fig. 6 on the same relative scale as a function of clock cycle (i.e., time) k. Interestingly, a peak is found at the output of this differentiator 52 at that point where the first plateau in $|J(k)|^2$ starts. This is the

main reason why a peak detector algorithm is applied at the output of the differentiator.

The autocorrelation block 20 together with the differentiator 52 and the peak detector 54 will constantly peer the channel. When the peak detector 54 identifies an absolute maximum, the synchronizer will consider that a new frame has arrived and the carrier frequency offset estimator will be activated. Because of the noise (thermal, digital), the peak detection will not be a trivial task, i.e. a smart peak detection algorithm will be necessary in order to distinguish the absolute from the relative maxima.

Fig. 8 shows a more detailed block diagram of a particular implementation of the 54 peak detector.

The instantaneous peak detector 60 is composed of a comparator 70 and a counter 72. The present sample $J_{diff}(k)$ coming out from the differentiator 52 is compared with the last recorded maximum J_{max} that is stored in a register 74. As long as the sample $J_{diff}(k)$ is bigger than J_{max}, the register 74 storing J_{max} will be updated to contain the new sample $J_{diff}(k)$ as the latest maximum and the counter 72 will be reset.

If $J_{diff}(k)$ is smaller or equal than J_{max}, the counter 72 will be triggered and it will increase its count by one. If this situation remains until the counter 72 counts through its full range, the instantaneous peak detector 60 will generate a signal stating that a relative peak was found inside the counting scope of the counter 72. In the implementation of Fig. 8 a 4-bit counter is used, which makes a counting scope of 16.

The group peak detector 58 is used to detect falling slopes in $J_{diff}(k)$, and its main component is also a comparison block. If the group peak detector finds a falling edge at the same time as the instantaneous peak detector finds a relative peak, this means that the detected peak is actually an absolute peak.

In the group peak detector, the input signal $J_{diff}(k)$ is accumulated in groups of six samples (6-tuples) in an accumulator 78 and the present group is

compared with the previous one. If it is smaller, it means that the falling slope has started.

Figure 7 shows a detailed scheme of the several signals involved in the peak detection procedure. A signal FS (dashed line) is given by the group peak detector (falling slope detector). The signal FS is zero until shortly after a peak has occured in the signal $J_{diff}(k)$ (full line),which is shown here again as in Fig. 6. At this point it switches to the value 1. When $J_{diff}(k)$ is detected to increase again, the signal FS switches back to zero. A signal C indicates the value of the counter 72. The counter signal C exhibits an increasing slope after the detection of a peak in the signal $J_{diff}(k)$ until the full range of the counter is reached. After that, the signal C jumps back to zero.

A signal FD (fat full line) represents the point in time where a decision on the existence of a peak is taken. FD is zero and exhibits a short peak at the point the counter signal 72 reaches its full range and the signal FS indicates a falling slope.

We have to mention that a frame will be detected 16 samples after its actual starting point, i.e., the detection will occur in the middle of the first plateau in $|J(k)|^2$ (dotted line in Fig. 7). However, this fact does not pose any problem, and the reason for the same will be given in the next section, where we explain the carrier frequency offset estimation.

In the following, a device and method for carrier frequency offset estimation and correction are described with reference to Figs. 9 to 11.

During the RF down-conversion, the local oscillator (LO) normally is not exactly tuned to the expected frequency, but it will show some offset. As the different sub-carriers in an OFDM system overlap, any frequency offset in the receiver side may lead to significant Inter-Carrier-Interference (ICI). Once the synchronizer has been fired after frame detection, the next operation will be the estimation of this frequency offset. Here we recover the expression given in equation (1) for the autocorrelation $J(k)$, considering that

$$y_{OFF}(n) = y(n) \cdot e^{j2\pi f_\varepsilon \frac{\Delta f}{f_S} n} \qquad (2)$$

where $y_{OFF}(n)$ is the signal affected by a normalized frequency offset f_ε. This normalization is with respect to the channel spacing Δf in the OFDM signal, which is 312.5 kHz in the IEEE 802.11a standard. The parameter f_S is the inverse of the FFT time (f_S = 20 MHz in the standard under consideration). The signal $J(k)$ may then be rewritten as

$$J(k) = e^{-j2\pi f_\varepsilon \frac{\Delta f}{f_S} N_d} \cdot \sum_{l=0}^{N_{avg}-1} y^*(l-k) \cdot y(l-k-N_d) \qquad (3)$$

If y(n) is a periodic signal with a period of N_d samples, i.e. $y(n) = y(n-N_d)$, then (3) can be simplified to

$$J(k) = e^{-j2\pi f_\varepsilon \frac{\Delta f}{f_S} N_d} \cdot \sum_{l=0}^{N_{avg}-1} |y(l-k)|^2 \qquad (4)$$

From equation (4) it can be seen that the phase of $J(k)$ is only due to f_ε, and so f_ε could be found as follows

$$f_\varepsilon = \frac{f_S}{2\pi \cdot N_d \cdot \Delta f} \tan^{-1}\left(J^*(k)\right) \qquad (5)$$

However, there are several factors which destroy the periodicity, making $y(n) \neq y(n-N_d)$. The most important ones are the AGC settling time and the channel impulse response. Another factor is noise, but its effect can be largely compensated by the averaging N_{avg} in equation (4). In addition, if N_{avg} is a multiple of the minimum periodicity in the preambles (16 samples in this standard), $|J(k)|^2$ shows a plateau in the region where the phase of $J(k)$ only depends on the carrier frequency offset.

Considering what has been stated above, the frequency offset is in the present embodiment estimated after calculation of the phase of $J(k)$, at that

point k where the peak detector established the beginning of the frame, because this point falls exactly in the middle of the plateau in $|J(k)|^2$.

Nevertheless, there is a limitation in the frequency offset estimation, which can be obtained by calculating the phase in the expression of equation (4), i.e.

$$-\pi \leq 2\pi f_\varepsilon \frac{\Delta f}{f_S} N_d < \pi \qquad (6)$$

The ratio $\Delta f / f_S$ is 1/64 in the IEEE 802.11a standard. From (6) it can be seen that the range of possible estimated values for f_ε will only depend on the selected delay N_d in the autocorrelator.

Figure 9 shows the dependency of the phase of $J^*(k)$ (conjugate value of $J(k)$) with respect to the input carrier frequency offset f_ε (normalized) for two particular values of N_d. Afterwards these two values will be used to obtain two estimations for the frequency offset, α and β.

In our implementation, f_ε is supposed to have its value in the range ± 1.5, i.e. a frequency offset of ± 468.75 kHz in an oscillator working in the 5 GHz ISM band. If the oscillator is tuned at 5.6 GHz, this value of expected offset is about 85 ppm (parts-per-million).

We will estimate f_ε decomposing its value into two components α and β, and the actual estimation ε will be a function of these two components, i.e. $\varepsilon = f(\alpha,\beta)$. The value of α is restricted to be in the range ± 0.5, and so is called the *fine frequency offset*. The parameter β is called *coarse frequency offset*, and it will be in the range ± 2.0 (see Figure 9). Our aim is to get proper estimations for these two parameters and combine them to finally obtain ε. With the presented scheme used for frame detection it is possible to derive the value for α.

Figure 10 shows an embodiment of a device 80 for frequency offset estimation and correction, which is based on the principles outlined above. In this device

two delayed autocorrelators 20 and 82 are used. Both are used for the frequency offset estimation, but only autocorrelator 20 of Fig. 1 (with N_d=64) is also used for the frame detection. Autocorrelator 82 uses the signal after a delay of N_d=16 .

We may estimate the value for α by calculating the phase an output of this autocorrelator 20, $J_F(k)$, which is the signal obtained before calculation its square amount. The estimation of β can be obtained using autocorrelator 82 with N_d=16 and $N_{avg}=N_d$ and calculating also the phase of its output $J_C(k)$.

The blocks 84 and 86 used to obtain α and β perform an *arctangent* calculation. This complex mathematical operation can be efficiently realized by using the CORDIC algorithm working in the *vectoring mode*. Although two arctangent blocks have been shown in Figure 10, only one is necessary in the actual implementation. After the frame has been detected by the peak detector 50, the two samples $J_C(k)$ and $J_F(k)$ will be stored in a register (not shown). The arctangent block 84, 86 will first calculate α from $J_F(k)$ and afterwards β from $J_C(k)$. More details on the CORDIC algorithm and its implementation can be found in the German Patent 101 64 462.0.

The correction of the frequency offset is carried out considering the signal model given in eq. (2). To obtain the original signal y(n), the input signal $y_{OFF}(n)$ has to be multiplied by a phasor, which is the complex conjugate of the one found in eq. (2). This operation will be carried out by a Numerically Controlled Oscillator (NCO) 122, cf. Fig. 17, which is implemented using again the CORDIC algorithm, this time operating in the *rotational mode*.

The dependency of α and β vs. f_s was sketched in Figure 9. There it can be seen that this dependency is not completely lineal, but shows some discontinuities. The reason for these discontinuities are the phase leaps from $+\pi$ to $-\pi$ at the complex exponential in eq. (4). Thus, the final value for ε cannot be a linear combination of the two estimations α and β. Thus one has to find a suitable way to combine α and β in order to determine ε.

From Figure 9 it can also be seen that β has no discontinuities throughout the entire range of expected values for f_ε (±1.5). Nevertheless, β will be much more noisy than α since the moving average considers only 16 samples (see Figure 10). For this reason, β will provide a coarse approximation of the frequency offset, which will be further refined using α.

The selected function ε=f(α,β) is as follows

$$\begin{aligned}
&\varepsilon=\alpha && ;\ \text{if } (-0.1)/4 \le \beta \le (0.1)/4 && \text{(R1)}\\
&\varepsilon=\alpha && ;\ \text{if } \alpha \ge 0 \text{ and } (0.1)/4 < \beta < (0.9)/4 && \text{(R2)}\\
&\varepsilon=1+\alpha && ;\ \text{if } \alpha < 0 \text{ and } (0.1)/4 < \beta < (0.9)/4 && \text{(R3)}\\
&\varepsilon=1+\alpha && ;\ \text{if } \beta \ge (0.9)/4 && \text{(R4)}\\
&\varepsilon=\alpha && ;\ \text{if } \alpha < 0 \text{ and } (-0.9)/4 < \beta < (-0.1)/4 && \text{(R5)}\\
&\varepsilon=-1+\alpha && ;\ \text{if } \alpha \ge 0 \text{ and } (-0.9)/4 < \beta < (-0.1)/4 && \text{(R6)}\\
&\varepsilon=-1+\alpha && ;\ \text{if } \beta \le (-0.9)/4 && \text{(R7)} \qquad (7)
\end{aligned}$$

In an alternative embodiment, the selected function is as follows:

$$\begin{aligned}
&\varepsilon=\alpha && ;\ \text{if } (-0.25)/4 \le \beta \le (0.25)/4 && \text{(R1)}\\
&\varepsilon=\alpha && ;\ \text{if } \alpha \ge 0 \text{ and } (0.25)/4 < \beta < (0.75)/4 && \text{(R2)}\\
&\varepsilon=1+\alpha && ;\ \text{if } \alpha < 0 \text{ and } (0.25)/4 < \beta < (0.75)/4 && \text{(R3)}\\
&\varepsilon=1+\alpha && ;\ \text{if } \beta \ge (0.75)/4 && \text{(R4)}\\
&\varepsilon=-1+\alpha && ;\ \text{if } \alpha \ge 0 \text{ and } (-0.75)/4 < \beta < (-0.25)/4 && \text{(R5)}\\
&\varepsilon=\alpha && ;\ \text{if } \alpha < 0 \text{ and } (-0.75)/4 < \beta < (-0.25)/4 && \text{(R6)}\\
&\varepsilon=-1+\alpha && ;\ \text{if } \beta \le (-0.75)/4 && \text{(R7)} \qquad (8)
\end{aligned}$$

Figures 11a) and b) show the different decision regions for the combination of α and β in the frequency offset estimation and correction. In this expression, certain regions R1 to R7 have been defined for different values of α and β, which are also indicated in Figs. 11a) and b). The estimation ε of the frequency offset will be assigned in combination block 88 depending on these particular regions.

In the following paragraphs, an example of a method and device for symbol timing estimation will be described.

Unlike to what was done during carrier frequency offset estimation, where the periodicity of the *short preamble symbols* was the main feature used for the estimation, the symbol timing estimation will be obtained by exploiting the direct knowledge of the *long preamble symbols* 12 and 14. After the frame is detected, the synchronizer knows approximately which samples of the preamble have entered the delay line of the autocorrelator 20, but this knowledge is not enough for further processing and has to be refined.

The main block of the symbol timing estimator is a crosscorrelator, cf. Fig. 17. Its main purpose is to compare the input frame with a reference signal, which is directly obtained from the long preamble symbol. The crosscorrelation can only be applied once the samples of the input frame have been corrected for the frequency offset by the NCO.

Figure 12 shows a timing diagram of the whole synchronization procedure. This is important to show at which point the input frame has been already corrected for the frequency offset. Only when this correction is done to the input frame, the crosscorrelator can be used for the timing estimation. The figure shows also the portion of the long preamble symbols used as reference signal in the crosscorrelator. The "piece" of the long preamble symbols selected as the crosscorrelator reference $c_{REF}(n)$ is shown in Figure 12. The reference has a length of 32 complex samples, which is the shortest possible length for this reference in order to obtain appropriate results after crosscorrelation.

Considering the standard IEEE 802.11a, the reference is as follows: $c_{REF}(0..31)$ = {0.1563, –0.0051–*j*0.1203, 0.0397–*j*0.1112, 0.0968+*j*0.0828, 0.0211+*j*0.0279, 0.0598–*j*0.0877, –0.1151–*j*0.0552, –0.0383–*j*0.1062, 0.0975–*j*0.0259, 0.0533+*j*0.0041, 0.0010–*j*0.1150, –0.1368–*j*0.0474, 0.0245–*j*0.0585, 0.0587–*j*0.0149, –0.0225+*j*0.1607, 0.1192–*j*0.0041, 0.0625–*j*0.0625, 0.0369+*j*0.0983, –0.0572+*j*0.0393, –0.1313+*j*0.0652, 0.0822+*j*0.0924, 0.0696+*j*0.0141, –0.0603+*j*0.0813, –0.0565–*j*0.0218, –0.0350–*j*0.1509, –0.1219–*j*0.0166, –0.1273–*j*0.0205, 0.0751–*j*0.0740, –0.0028+*j*0.0538, –0.0919+*j*0.1151, 0.0917+*j*0.1059, 0.0123+*j*0.0976}, where $j=\sqrt{-1}$.

From the implementation point of view, the complex crosscorrelator is usually a "weak" point in modern communication circuit designs because of its computation complexity (they require a large number of complex multipliers) and subsequent need for large silicon area. Having this in mind, in this implementation we used a simplified scheme for the crosscorrelator, based on simple XNOR 1-bit multipliers (Figure 13), that substitute the commonly used complex multipliers.

Figure 13 shows a scheme of an XNOR-based complex multiplier. The multiplier comprises four XNOR-gates 90 to 96 The two signals to be multiplied are $A=A_{real}+jA_{imag}$ and $B=B_{real}+jB_{imag}$, with $j=\sqrt{-1}$. Both real and imaginary parts are only one bit long, i.e. '1' if the signal is positive and '0' if it is negative. Thus, instead of multiplying N-bit complex numbers, the XNOR multiplier of Fig. 13 performs only the multiplication of the sign bits of the complex input values.

In the following, the use of XNOR multipliers for complex multiplication is explained in more detail:

The multiplication of two complex numbers $A = A_{real} + j\ A_{imag}$, and $B = B_{real} + j\ B_{imag}$, where $j = sqrt(-1)$, results in $C = A \times B$, which is also complex with $C_{real} = (A_{real} \times B_{real}) - (A_{imag} \times B_{imag})$and $C_{imag} = (A_{imag} \times B_{real}) + (A_{real} \times B_{imag})$

This means that in principle four multipliers 90 to 96 and two adders 98 and 100 are necessary.

In this case, the multiplication of A_{real} x B_{real} may comprise the following possible combinations:

A_{real}	B_{real}	A_{real} x B_{real}
0	0	1
0	1	0
1	0	0
1	1	1

This table is equivalent to a XNOR gate with inputs A_{real} and B_{real}, i.e., this gate produces a '0' at the output when the number of '1' inputs is odd.

The previous operation has to be repeated 4 times in a complex multiplication. As mentioned before, in the present embodiment we represent A_{real}, A_{Imag}, B_{real} and B_{imag} with a single bit, i.e., if they are positive we use a '1' whereas when negative we use a '0'. Let dA_{real}, dA_{imag}, dB_{real}, dB_{imag}, dC_{real} and dC_{imag} be the representation of A_{real}, A_{imag}, B_{real}, B_{imag}, C_{real} and C_{imag} by a single bit, respectively. Now the value of dC_{real} and dC_{imag} is:

$$dC_{real} = XNOR(dAreal, dBreal) - XNOR(dAimag, dBimag)$$

$$dC_{imag} = XNOR(dAimag, dBreal) + XNOR(dAreal, dBimag)$$

An important point to be noted is that the original signals A_{real}, B_{real}, A_{imag} and B_{imag} may take positive or negative values, but they have no DC level, i.e., on the average they are positive and negative the same amount of time. When

converting them into '1' or '0' a DC level is introduced which is going to be 0.5. After the XNOR operation, the non-zero DC offset still will be present. Nevertheless this is not a problem when calculating dC_{real} because the DC levels get compensated due to the subtraction operation. But for the case of dC_{imag}, both DC levels are accumulated. For this reason in Figure 13 of the there is a DC level subtraction 101.

In addition, a further simplification in the structure of these multipliers is possible if one of the inputs is fixed and is known beforehand. The simplified structure of multipliers based on this knowledge is shown in Fig. 14 (A) to Fig. 14(D). Figure 14 shows possible simplifications of the XNOR-based complex multiplier if the input B is known a priori. In this simplification, the XNOR gates may be replaced by NOT gates, which require a less number of transistors.

If the value of B is known beforehand, only two rows in the previous logic table are to be considered. There are four possible cases: $dB_{real}=0$, $dB_{imag}=0$; $dB_{real}=1$, $dB_{imag}=1$; $dB_{real}=1$, $dB_{imag}=0$; $dB_{real}=0$, $dB_{imag}=1$. In this case the XNOR gates are simplified to NOT gates, which require a smaller number of transistors.

Considering an example dA_{real} x dB_{real} knowing already that dB_{real} = '0', according to the previous table, the result of the multiplication is the inverse of the input. This means that no XNOR gate is needed but just a NOT gate, such as for example NOT gate 102 in Fig. 14 (A). On the other hand, if dB_{real} is known to be '1', the previous table says that the result of the multiplication is directly the input value dA_{real}. Here, no gate is required at all, cf. for example Fig. 14 (B). The multipliers of Figs 14 (C) and (D) are built using similar considerations.

The final results dC_{real} and dC_{imag} are represented by 2 bits each. For comparison, if A_{real}, B_{real}, A_{imag} and B_{imag} were coded by for instance 16 bits, C_{real} and C_{imag} would comprise 32 bits if a full multiplication would have been used.

The final structure of a crosscorrelator 108 based on these principles is shown in Figure 15. It is composed of 32 delay elements 110 and 32 multipliers 112. The structure of each multiplier 112 is chosen in dependence on the reference signal $c_{REF}(31,..,0)^*$, where we already considered the reference to be complex conjugated, hard-limited and order-reversed. The final reference looks as follows

$c_{REF}(31,..,0)^*$={1, 1, 0, 0, 1+*j*, *j*, *j*, *j*, *j*, 0, 1, 1, 0, 0, 1, 1+*j*, 1+*j*, 0, 1+*j*, 1+*j*, *j*, 1+*j*, 1, 1+*j*, *j*, *j*, 1+*j*, 1, 1, 1+*j*, *j*, 1}, where $j=\sqrt{-1}$.

The multiplication signals are added in and adder 114. The square magnitude of the output of adder 114 is calculated in a block 116.

The output of the crosscorrelator 108 is shown in Figure 16 as a function of the numbers of clock cycles n, i.e., as a function of time. Two major peaks P1 and P2 become visible at instants n_{init1} and n_{init2}. Both peaks P1 and P2 will occur when the portions AB in the long preamble symbols (see Figure 12) are inside the crosscorrelator 108. For our purpose it is sufficient to detect the first peak P1 by setting a certain threshold at the output of the crosscorrelator 108. The 64 samples coming immediately after this first peak will be fed into an FFT block (CDAB fields marked with "First FFT symbol" in Figure 12) in order to get the *reference channel estimation*.

The following description concerns the step of reference channel extraction. The reference channel estimation is used by the channel estimator in order to correct for the filtering due to the transmission channel. The reference channel will be obtained by calculating the FFT of the CDAB fields in Figure 12. This operation is performed by an FFT block 120 (cf. Fig. 17) and may start immediately after the crosscorrelator 108 decides the initial timing n_{init1}. Nevertheless, the resulting FFT calculation has to be multiplied by the sequence $(-1)^m$, m being the frequency variable.

In the IEEE 802.11a standard, the actual long preamble symbols are defined as ABCD, i.e. a cyclic delay of 32 samples into a sequence of 64 samples is

introduced. After performing the FFT, any time delay is seen as a linear phase, which in this specific case is reduced to the sequence $\exp\{-j2\pi(32/64)m\}=\exp\{-j\pi m\}=(-1)^m$. In order to compensate for this linear phase, the FFT output has to be multiplied exactly by this sequence.

The phase compensation mentioned above is only necessary when calculating the reference channel estimation. For the data symbols coming after the preamble no phase correction will be necessary.

Figure 17 shows a general synchronizer scheme with different clock domains. Each clock domain is activated when it has to carry out some kind of operation. If not, it is disabled in order to reduce the power consumption of the whole synchronizer. The clock domains are indicated by different hatches in Fig. 17. A first clock domain comprises the autororrelators 20 and 82 (cf. also Fig. 10), peak detector 50, and the arctan-block 84/86. A second clock domain comprises NCO 122 and FFT block 120. A third clock domain includes crosscorrelator 108.

There are two further operations to be performed inside the FFT block 120 in Figure 17. As the synchronizer already knows the timing of the input samples, it can detect the end of the preamble symbols and the beginning of the data symbols. The data symbols will go through a *cyclic prefix* extraction block (not shown) prior to the FFT calculation. The cyclic prefix extraction is mainly formed by a counter. For each data symbol, 80 samples are expected. The first 16 will be discarded and the last 64 will be fed into the FFT block 120. The cyclic prefix is inserted in the OFDM symbols in order to prevent the Inter-Symbol-Interference (ISI) caused by the channel filtering.

The last operation included inside the FFT block 120 is the channel reordering. Immediately after the FFT calculation, the output samples are delivered in the serial form according to the natural order. For further processing, this order has to be changed. Specifically, the data after FFT is given in the following order: D_0, D_1, D_2, ..., D_{31}, D_{-32}, D_{-31}, D_{-30}, ..., D_{-1}, where the subindex indicates the corresponding sub-channel. But the samples D_0,

D_{27}, D_{28}, D_{29}, D_{30}, D_{31}, D_{-32}, D_{-31}, D_{-30}, D_{-29}, D_{-28} and D_{-27} (11 samples in total) carry no information and are directly discarded. The remaining 52 samples $\{D_k / k \in [1,26] \cup [-26,-1]\}$ are provided at the output of the FFT block 120 in the following order: D_{-21}, D_{-7}, D_7, D_{21}, D_{-26}, D_{-25}, ..., D_{-22}, D_{-20}, D_{-19}, D_{-18}, ..., D_{-8}, D_{-6}, D_{-5}, ..., D_{-1}, D_1, ..., D_5, D_6, D_8, ..., D_{18}, D_{19}, D_{20}, D_{22}, ..., D_{25}, D_{26}.

The actual implementation of the FFT processor 120 itself is not going to be explained in detail here. The main idea behind this implementation has been a mathematical manipulation of the definition of the FFT in order to convert the 64-point FFT into a 2-dimensional 8x8-point FFT. For more details see the German Patent application DE 100 62 759.5.

Figure 18 shows a representation of the two operation modes of the circular CORDIC algorithm being used in the synchronizer.

The CORDIC processor is a part of the synchronizer. The processor performs the circular CORDIC algorithm in both of its operation modes, viz. *rotational* and *vectoring*. While the rotation mode of operation of the CORDIC enables us to compute the multiplication of any quantity with a phasor $\exp\{j\varphi\}=\cos(\varphi)+j\sin(\varphi)$, the vectoring mode can be used for computing the magnitude and the phase angle of a complex value. The operation principle of these two modes is shown in Figure 18.

The rotational mode is useful to implement the NCO 122 whereas, the vectoring mode is useful for arctangent calculations in block 84,86. However, for the realization of the synchronizer, these two modes of operation of the CORDIC are independently utilized in two different phases. At first, the phases of $J_F(k)$ and $J_C(k)$ (see Figure 10) are computed (vectoring mode of operation) to obtain α and β, respectively. After calculation of ε by combining α and β, this phase angle is used to obtain a phase correction for the incoming data symbols applying a numerically controlled oscillator (NCO) 122 in the rotation mode of operation. The phase angle evaluation takes place only once at the beginning of the frame (after frame detection) whereas, for the rest of the frame the NCO operation is carried out. Thus, in our consideration, it is more

pragmatic to separate the two modes of CORDIC operation and realize them in the form of two separate modules. This separation of operations opens up the possibility for applying clock gating to save the power corresponding to the NCO 122 while the computation of the phase angle is carried on and vice versa. On the other hand, this separation results in a massive reduction of control hardware as no reuse of the component takes place that subsequently eliminates any feedback path. Another advantage of separating these two functionalities is that, in this case, it is possible to implement each of them in a much simplified and efficient manner.

When using the rotational CORDIC as an NCO, the input signal is multiplied by a phasor with the form $\exp\{j(2\pi/64)\cdot\varepsilon\cdot n\}$, where ε is the estimated normalized carrier frequency offset (see Figure 10) and n is the time variable. Thus, the variable φ in Figure 18.a depends on n, and it is updated at each clock cycle. This is done by adding a phase accumulator to the input φ in the CORDIC processor.

We have to mention here that the value of ε must not be sign-reversed in order to apply a correct phase correction, because the result coming from the arctangent calculation already considers this sign. This can be easily seen in expression (4), where by definition, the phase contribution in $J(k)$ already contains the *–ve* sign.

The actual implementation of the rotational and vectoring CORDIC processors is described in more detail in the German Patent 101 64 462.0.

In summary, the the proposed synchronizer has the following advantages:

The proposed synchronizer has been designed as a power efficient system. This has been achieved in one side by optimizing each block independently and on the other side by dividing the whole synchronizer structure into different clock domains (see Figure 17).

A clock demain separation helps to save power in the sense that only certain regions of the system are activated for operation, while others are not, by

applying the *clock* gating. Thus, as shown in Figure 17, three clock domains are used here. The blocks belonging to the clock domain #1 peer the channel trying to detect an incoming frame through the peak detector algorithm. When this is true, the arctangent calculation is triggered, but it will operate only on two samples, thus obtaining two single values for α and β. Afterwards this clock domain is disabled. The combination of α and β to finally obtain ε can be done using combinatorial logic, thus requiring no clock at all.

Disabling the clock domain #1, it is possible to save the power that otherwise would be consumed by the huge delay line at the input of the autocorrelator as well as the FIR structures of the moving average blocks.

Once the value for ε is available, the NCO 122 will start its operation until the end of the frame. The crosscorrelator 108 will be activated at the same time, but it will operate only until a peak is found at its output, being afterwards disabled. This is achieved by assigning a particular clock domain to the crosscorrelator 108 (clock domain #3).

The FFT block 120 is activated after a peak is detected at the output of the crosscorrelator and will operate like the NCO 122, until the end of the incoming frame, for that reason both the NCO 120 and the FFT blocks 120 belong to the same clock domain #2.

Apart from the power saving in the system level by applying clock gating, even more power saving is achieved by optimising each single block in the synchronizer as described above.

Thus, the frame detection algorithm is based on the knowledge of the ideal shape of the signal $|J_F(k)|^2$. A simple and robust peak detection algorithm is applied to this signal in order to detect an incoming frame. The arctangent calculation as well as the NCO 122 are based on the CORDIC algorithm. The CORDIC processors designed for these purposes have been optimised to reach the final angle in an adaptive way and thereby executing a minimum number of iteration steps. Furthermore, the crosscorrelator has been simplified

to use XNOR-based complex multipliers instead of the normal complex multipliers and the reference signal therein has been shorten as much as possible in order to obtain valid results. Last but not least, the FFT processor 120 has been also optimised by using a new architecture, which requires no coefficient storing or complex multiplier.

The whole structure introduces a latency of 3.9 μs counted from the instant when the frame is detected. This value is less than one OFDM symbol period (4 μs), which means that no extra storage of the input samples has to be done inside the synchronizer.

In summary, there are the following inventions comprised in the above description:

The algorithm used for the frame detection, making use of a simplified differentiator to obtain an absolute maximum in the differentiated signal at that point where the first plateau in $J_F(k)$ starts (output of the autocorrelator with N_d=64);

The design of the peak detector to obtain the position of the absolute maximum in the differentiated signal, dividing the problem into relative peak detection and falling edge detection;

The way to combine the two frequency offsets α and β to finally obtain ε;

The use of a 32-sample long reference signal in the crosscorrelator for timing estimation;

The use of our simplified XNOR-based crosscorrelator, and the simplifications therein based on the knowledge of the reference;

The use of our particular solution for the CORDIC algorithm in the vectoring mode for arctangent calculation;

The use of our particular solution for the CORDIC algorithm as NCO for the frequency offset correction;

The hardware structuring of the whole synchronizer, allowing a very simple control mechanism and the separation of this structure into different clock domains, each one being activated only to perform its operation and deactivated afterwards.

The following is a table relating terms used in the present application to those used in European patent application 02 090 257.3, whose priority is claimed, with the same meaning.

Priority application	This application
third signal	autocorrelation signal
fourth signal	second signal
fifth signal	differentiator signal
sixth signal	instantaneous peak detection signal
seventh signal	group peak detection signal
eighth signal	maximum detection signal
first predetermined number N_d (claim 2)	third predetermined number N_d
second predetermined number N_{avg} (claim 3)	fourth predetermined number N_{avg}
third predetermined number (claim 8)	first predetermined number
fourth predetermined number (claim 14)	predetermined accumulation number
predetermined range of sampling periods (claim 7)	second predetermined number of sampling periods
transforming step (claims 1 and 2)	step b), autocorrelation step (claim1)

Claims

1. A method for the detection of the reception of a data frame in an input signal (y_{OFF} (n)), said data frame comprising periodically repeated symbols at the beginning, comprising the steps of

   a) sampling said input signal (y_{OFF} (n)) with a predetermined sampling rate,

   b) generating a first signal ($|J(k)|^2$) that is dependent on an autocorrelation of said input signal with a delayed copy of said input signal, and

   c) detecting a plateau in said first signal ($|J(k)|^2$)

   d) generating an output signal that is indicative of detecting said plateau.

   wherein said step of detecting a plateau comprises the steps of

   c1) generating a differentiator signal (J_{diff} (k)), which is dependent on the difference of a first sample of said first signal and a second sample of said first signal that was taken a first predetermined number of sampling periods earlier, and

   c2) detecting an absolute maximum of said differentiator signal (J_{diff} (k)) within a second predetermined number of sampling periods.

2. The method according to claim 1, wherein said step c2) of detecting an absolute maximum comprises an instantaneous peak detection step and a step of detecting a falling slope in the differentiator signal (J_{diff} (k)).

3. The method according to claim 2, wherein the instantaneous peak detection step and the group peak detection step are performed in parallel.

4. The method of claim 2 or 3, wherein the instantaneous peak detection step comprises a step of comparing the differentiator signal (J_{diff} (k)) of a current sampling period with the differentiator signal (J_{diff} (k)) of a next previous sampling period, and a step of saving the differentiator signal (J_{diff} (k)) of the current sampling period to a register, given the condition that its value is larger than that of the differentiator signal (J_{diff} (k)) of the previous sampling period.

5. A method according to claim 4, comprising a step of incrementing a count index by one, given the condition that the value of said differentiator signal (J_{diff} (k)) of said current sampling period is equal or smaller than that of said differentiator signal (J_{diff} (k)) saved in said register.

6. A method according to claim 5, comprising a step of generating an instantaneous peak detection signal indicative of the condition whether or not the count index has reached a predetermined count value.

7. A method according to claim 1, comprising a step of detecting a falling slope in said differentiator signal (J_{diff} (k)).

8. A method according to claim 7, wherein detecting a falling slope comprises the steps of

- generating an accumulation signal that is dependent on the sum of said differentiator signal (J_{diff} (k)) over a fourth predetermined number of consecutive sampling periods
- comparing said current accumulation signal with the last previous accumulation signal representing without overlap said fourth predetermined number of consecutive earlier sampling periods
- generating a group peak detection signal indicative of whether or not the value of said current accumulation signal is smaller than the value of said earlier accumulation signal.

9. A method according to claims 6 and 8, comprising a step of generating a maximum detection signal indicative of the condition

   - that said instantaneous peak detection signal indicates that the count index has reached the predetermined count value and

   - that said group peak detection signal indicates that the value of said current accumulation signal is smaller than said value of said earlier accumulation signal.

10. A method according to any one of the preceding claims, wherein said output signal is indicative of the time of detecting said plateau.

11. A method according to any one of the preceding claims, wherein said method is used for detecting a data frame containing OFDM symbols.

12. A method according to any one of the preceding claims, wherein the input signal is amplified such that the power of the amplified input signal is in a predetermined power range.

13. A method according to claim 1 or 12, wherein the step of detecting a plateau in said first signal ($|J(k)|^2$) is performed only if the first signal exceeds a predetermined threshold value.

14. A frame detector for detecting the reception of a data frame in an input signal ($y_{OFF}(n)$), said data frame comprising periodically repeated symbols at the beginning, comprising

   a) a sampling unit adapted to sample said input signal ($y_{OFF}(n)$) with a predetermined sampling rate

   b) an autocorrelation unit adapted to transform said input signal ($y_{OFF}(n)$) into a first signal ($|J(k)|^2$) that is dependent on an autocorrelation of said input signal with a delayed copy of said input signal, and

c) a plateau detector, adapted to detect a plateau in said first signal ($|J(k)|^2$)

d) an output unit adapted to generate an output signal that is indicative of detecting said plateau,

wherein said plateau detector is adapted to generate a differentiator signal (J_{diff} (k)), which is dependent on the difference of a first sample of said first signal and a second sample of said first signal a predetermined number of sampling periods earlier, to detect an absolute maximum of said differentiator signal (J_{diff} (k)) within a predetermined range of sampling periods, and to provide a signal indicative of detecting said absolute maximum to said output unit.

15. The frame detector of claim 14, wherein said plateau detector comprises a peak detection unit with

a) a first detection unit connected to said input port and comprising a first memory unit, said first detection unit being adapted to

- comparing said input signal (J_{diff} (k)) received through said input port with a first entry contained in said first memory unit, and to

- replacing said first entry by said input signal given the condition that the value of said input signal (J_{diff} (k)) is larger than the value of said first entry,

b) a second detection unit connected to said input port and comprising a second memory unit, said second detection unit being adapted to

- generating an accumulation signal, that is dependent on the sum of a current input signal (J_{diff} (k)) and of said fourth predetermined number of previous input signals (J_{diff} (k)),

- comparing said accumulation signal with a second entry contained in said second memory for at least , and to

- replacing said second entry by said accumulation signal given the condition that the value of said accumulation signal (J_{diff} (k)) is larger than the value of said second entry,

said peak detection unit being adapted to providing a peak detector output signal at its output port indicative of whether or not said first entry has been unchanged for a predetermined number of sample periods and said second entry has been changed in said current sampling period.

16. A synchronizing method comprising a step of detecting a frame in an input signal, wherein the frame detection step is performed with the method of at least one of the claims 1 to 11.

17. A synchronizing method according to claim 16, further comprising a step of estimating a relative frequency offset (f_ε) in an input signal ($y_{OFF}(n)$) after said step of detecting a frame, wherein the estimating step comprises the steps of

a) estimating a coarse frequency offset (β)

b) estimating a fine frequency offset (α) in dependence of said estimated coarse frequency offset (β).

18. The synchronizing method of claim 17, wherein the steps of estimating a coarse frequency offset (β) or of estimating a fine frequency offset, or both steps, comprise a step of calculating a phase value of said first signal ($|J(k)|^2$).

19. The synchronizing method of claim 17 or 18, wherein the step of estimating the frequency offset comprises a step of assigning a fine frequency offset value dependent on the value of the coarse frequency offset according to the following function:

$\varepsilon=\alpha$; if $(-0.25)/4 \leq \beta \leq (0.25)/4$ (R1)

$\varepsilon=\alpha$; if $\alpha \geq 0$ and $(0.25)/4 < \beta < (0.75)/4$ (R2)

$\varepsilon=1+\alpha$; if $\alpha < 0$ and $(0.25)/4 < \beta < (0.75)/4$ (R3)

$\varepsilon=1+\alpha$; if $\beta \geq (0.75)/4$ (R4)

$\varepsilon=-1+\alpha$; if $\alpha \geq 0$ and $(-0.75)/4 < \beta < (-0.25)/4$ (R5)

$\varepsilon=\alpha$; if $\alpha < 0$ and $(-0.75)/4 < \beta < (-0.25)/4$ (R6)

$\varepsilon=-1+\alpha$; if $\beta \leq (-0.75)/4$ (R7)

20. The synchronizing method of claim 17 or 18, wherein the step of estimating the frequency offset comprises a step of assigning a fine frequency offset value dependent on the value of the coarse frequency offset according to the following function:

$\varepsilon=\alpha$; if $(-0.1)/4 \leq \beta \leq (0.1)/4$ (R1)

$\varepsilon=\alpha$; if $\alpha \geq 0$ and $(0.1)/4 < \beta < (0.9)/4$ (R2)

$\varepsilon=1+\alpha$; if $\alpha < 0$ and $(0.1)/4 < \beta < (0.9)/4$ (R3)

$\varepsilon=1+\alpha$; if $\beta \geq (0.9)/4$ (R4)

$\varepsilon=\alpha$; if $\alpha < 0$ and $(-0.9)/4 < \beta < (-0.1)/4$ (R5)

$\varepsilon=-1+\alpha$; if $\alpha \geq 0$ and $(-0.9)/4 < \beta < (-0.1)/4$ (R6)

$$\varepsilon = -1+\alpha \quad ; \text{if } \beta \leq (-0.9)/4 \qquad \text{(R7)}$$

21. The synchronizing method of one of the claims 16 to 20, further comprising a step of correcting the input signal by the estimated value.

22. The synchronizing method of claim 21, further comprising after said step of frequency offset correction a step of estimating the time of reception of at least one symbol contained in a received data frame (hereinafter symbol timing step).

23. The synchronizing method of claim 22, wherein the symbol timing step comprises a step of generating a crosscorrelation signal, which is dependent on the value of the crosscorrelation of the corrected input signal with a known reference signal, wherein the reference signal is a first section of long preamble symbols included in the data frame.

24. The synchronizing method of claim 23, wherein the reference signal is 32 samples long.

25. The synchronizing method of one of the claims 22 to 24, further comprising a step of estimating a reference channel.

26. The synchronizing method of claim 25, wherein estimating the reference channel comprises a step of performing a Fast Fourier Transform of a second section of the long preamble symbols included in the data frame.

27. A synchronizer device comprising a frame detector according to claim 14 or 15.

28. The synchronizer device of claim 27, further comprising a symbol timing unit adapted to generate a crosscorrelation signal, which is dependent on the value of the crosscorrelation of the corrected input signal with a known reference signal, wherein the reference signal is a first section of long preamble symbols included in the data frame.

29. The synchronizer device of claim 28, wherein the symbol timing unit comprises a crosscorrelation unit with a number of multipliers for complex numbers, and wherein at least one multiplier is made of a combination of XNOR-gates, inverter gates and adders.

30. The synchronizer device of one of the claims 27 to 29, wherein the frame detection unit and the symbol timing unit can be enabled or disabled individually.

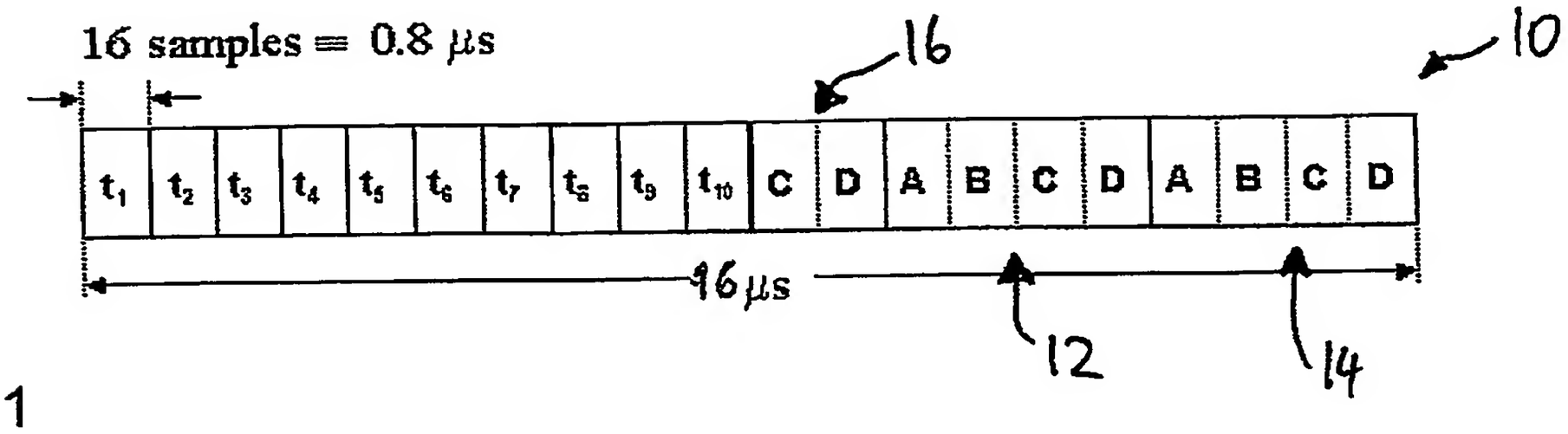


Fig. 1

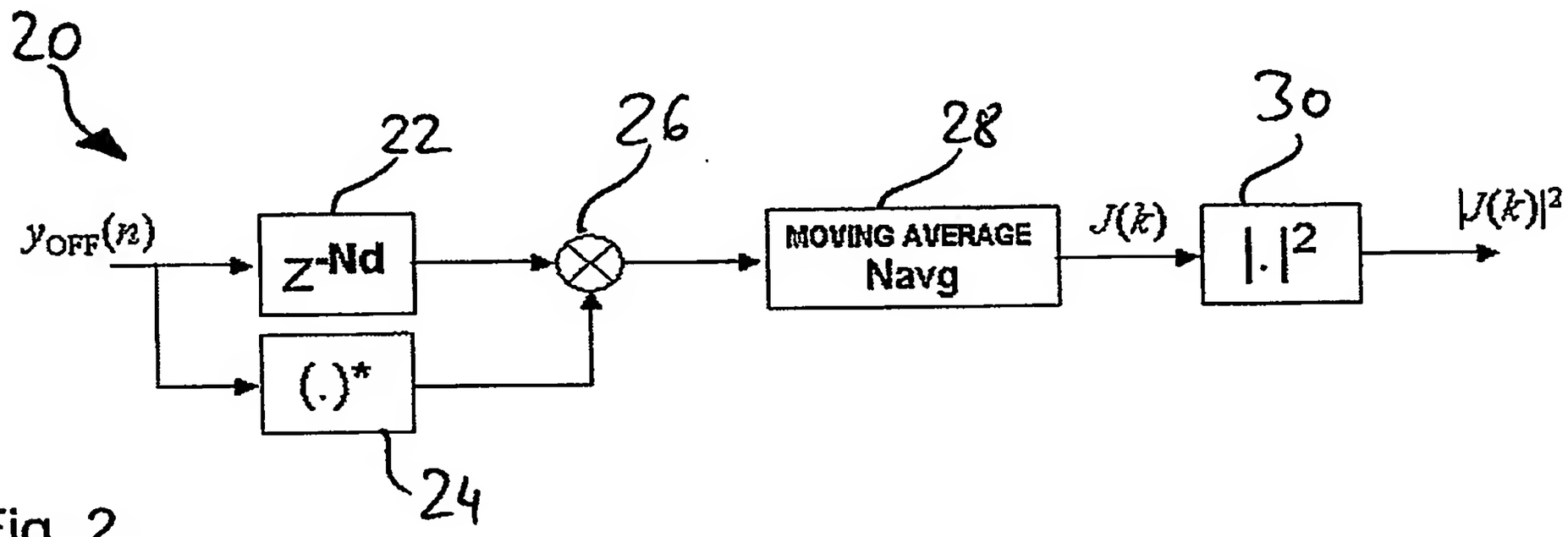


Fig. 2

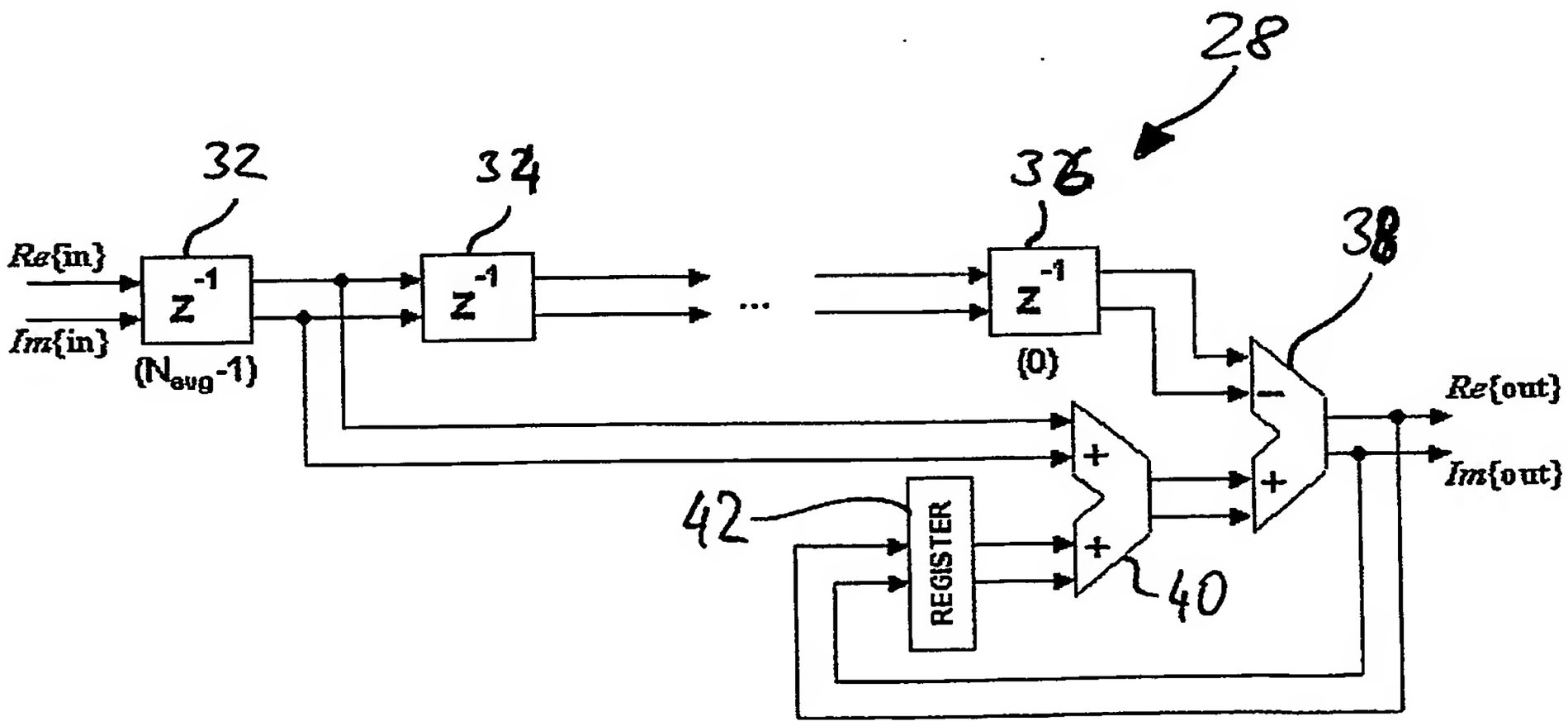
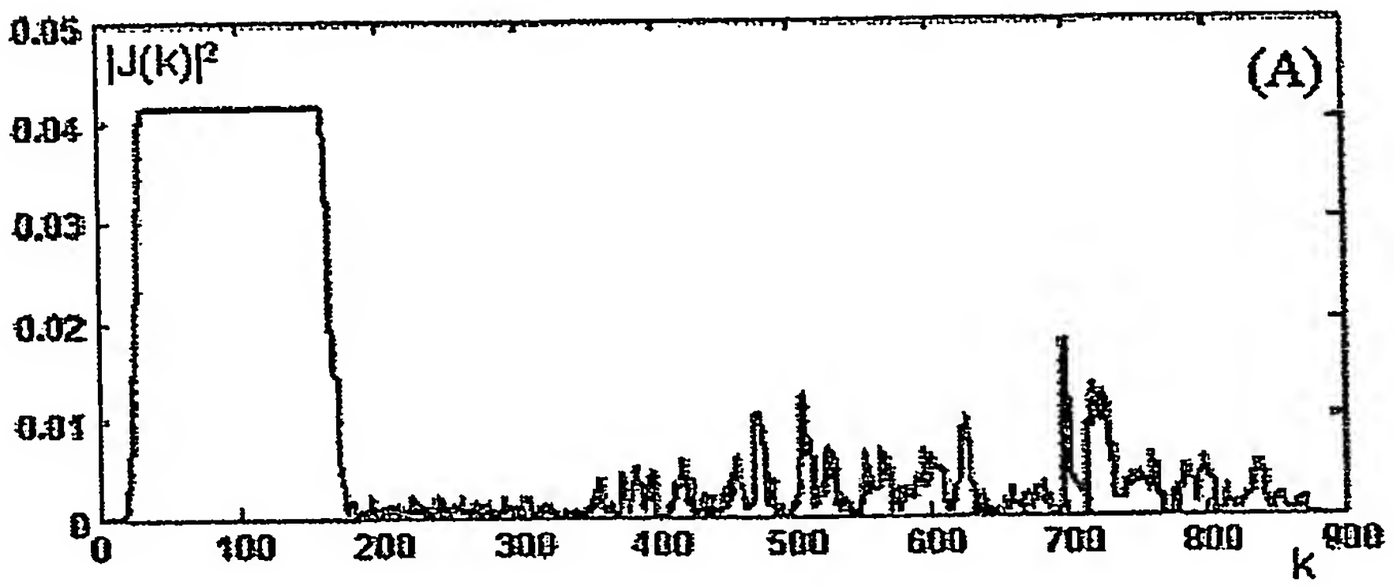


Fig. 3


|J(k)|²
(A)
0.05
0.04
0.03
0.02
0.01
0
0
100
200
300
400
500
600
700
800
900
k

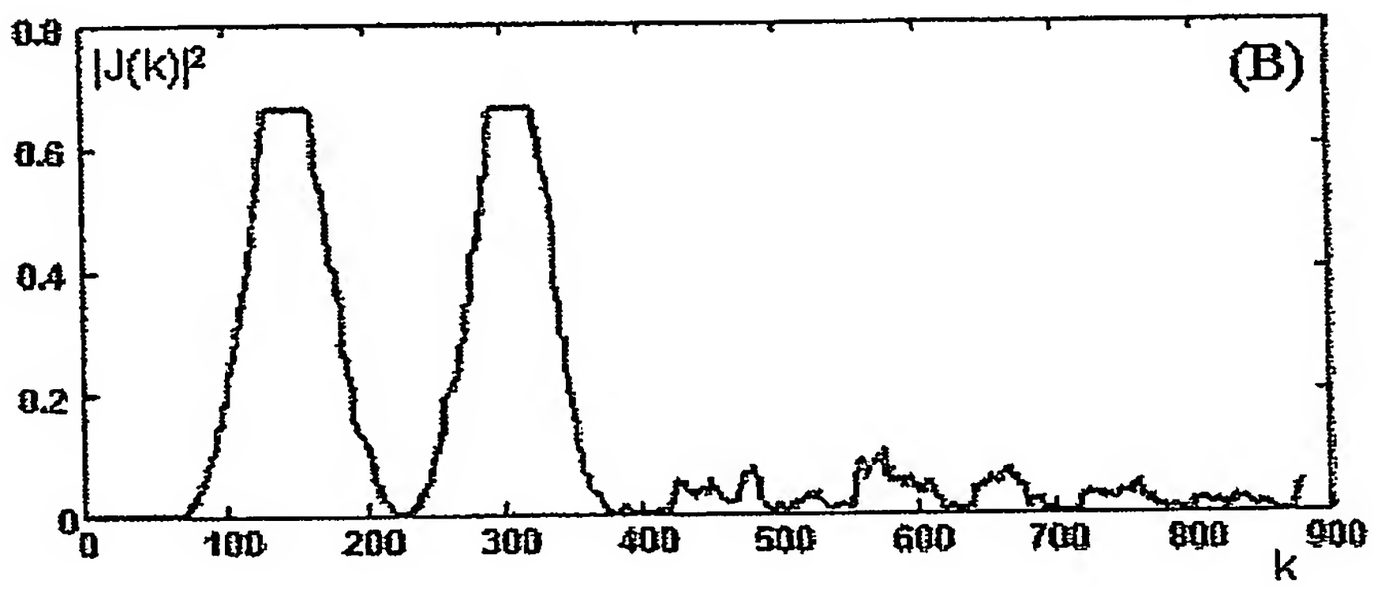

|J(k)|²
(B)
0.8
0.6
0.4
0.2
0
0
100
200
300
400
500
600
700
800
900
k

Fig. 4

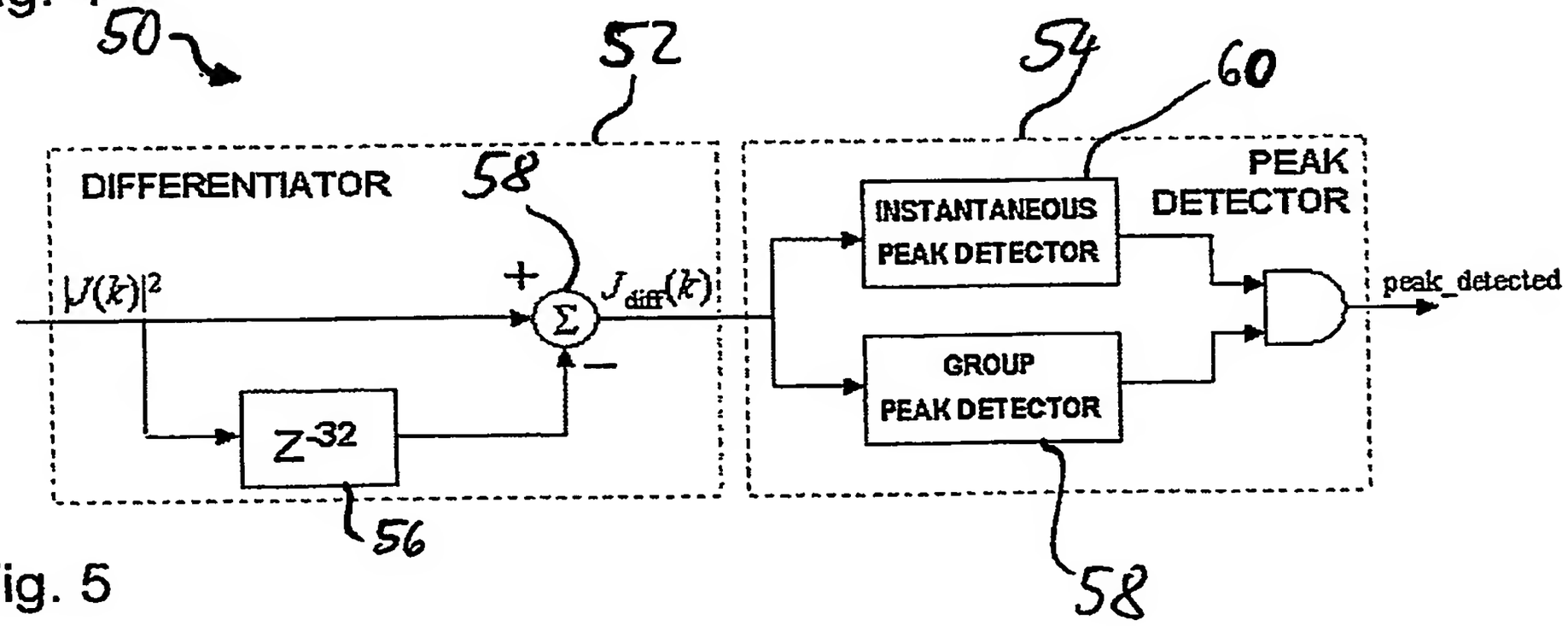

50
52
54
60
DIFFERENTIATOR
58
PEAK DETECTOR
INSTANTANEOUS PEAK DETECTOR
GROUP PEAK DETECTOR
|J(k)|²
+
Σ
−
J_diff(k)
Z^-32
peak_detected
56
58

Fig. 5

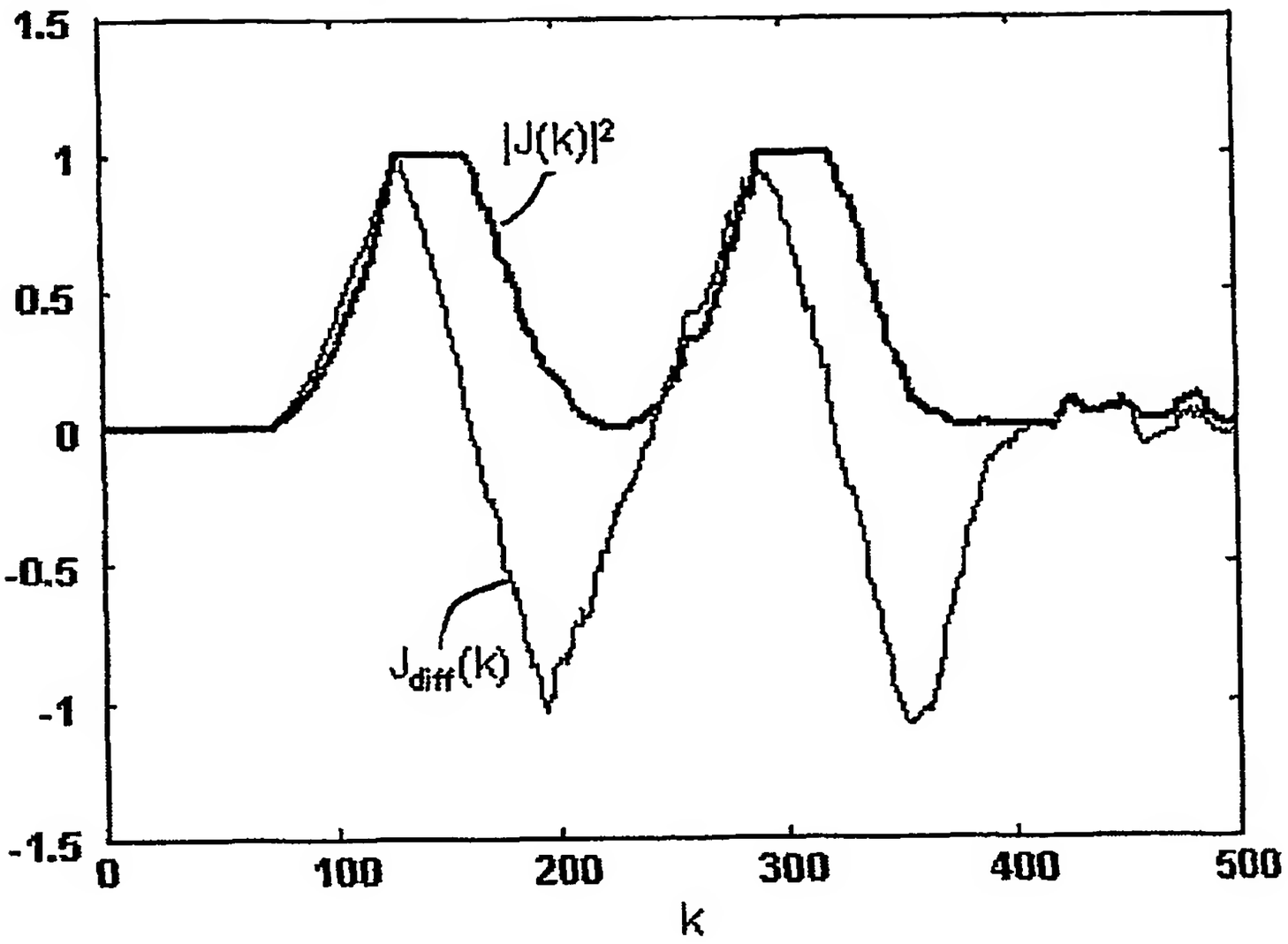

1.5
1
0.5
0
-0.5
-1
-1.5
0
100
200
300
400
500
k
|J(k)|²
J_diff(k)

Fig. 6

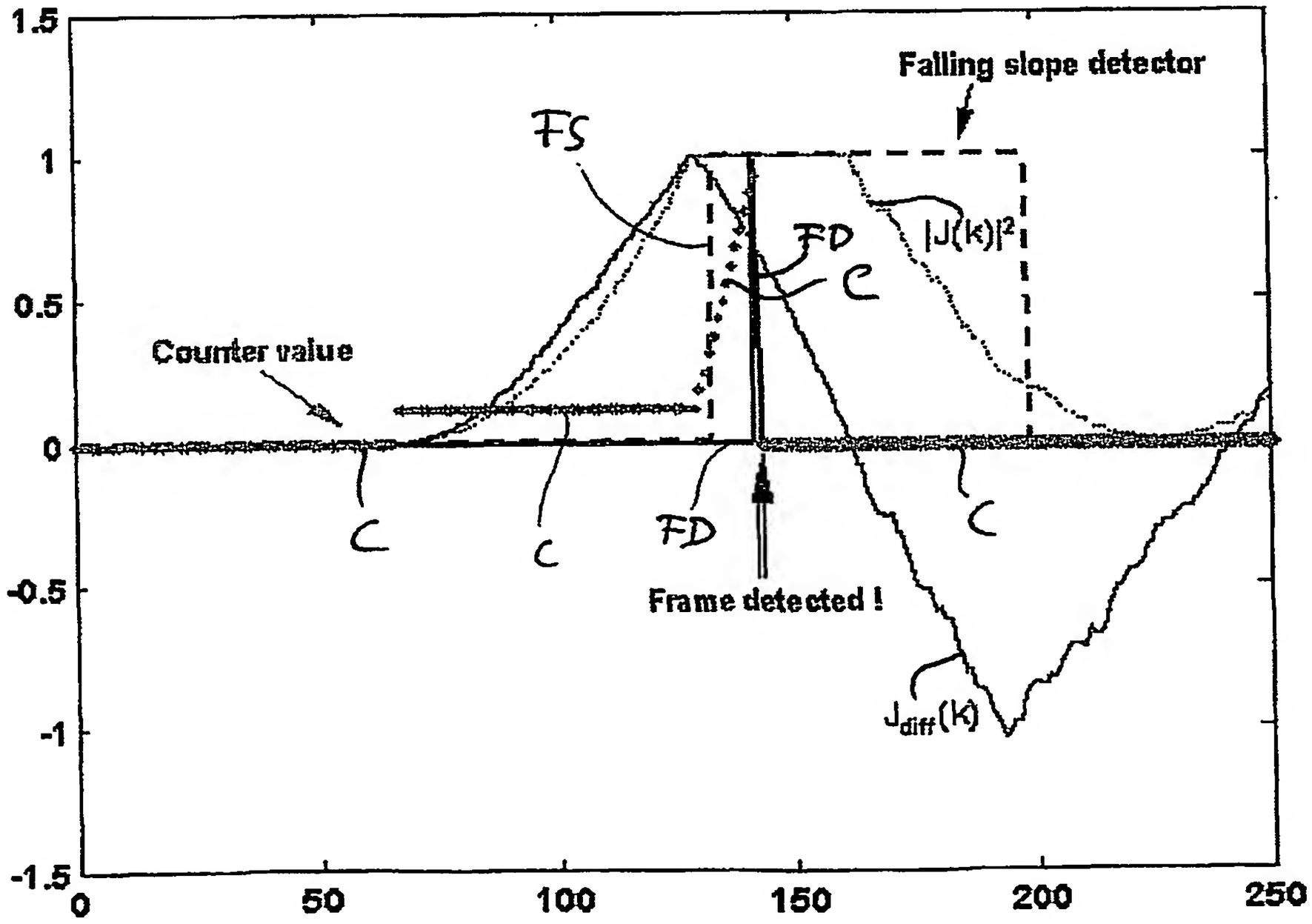

1.5
1
0.5
0
-0.5
-1
-1.5
0
50
100
150
200
250
Falling slope detector
FS
FD
C
|J(k)|²
Counter value
C
C
FD
Frame detected !
C
J_diff(k)

Fig. 7

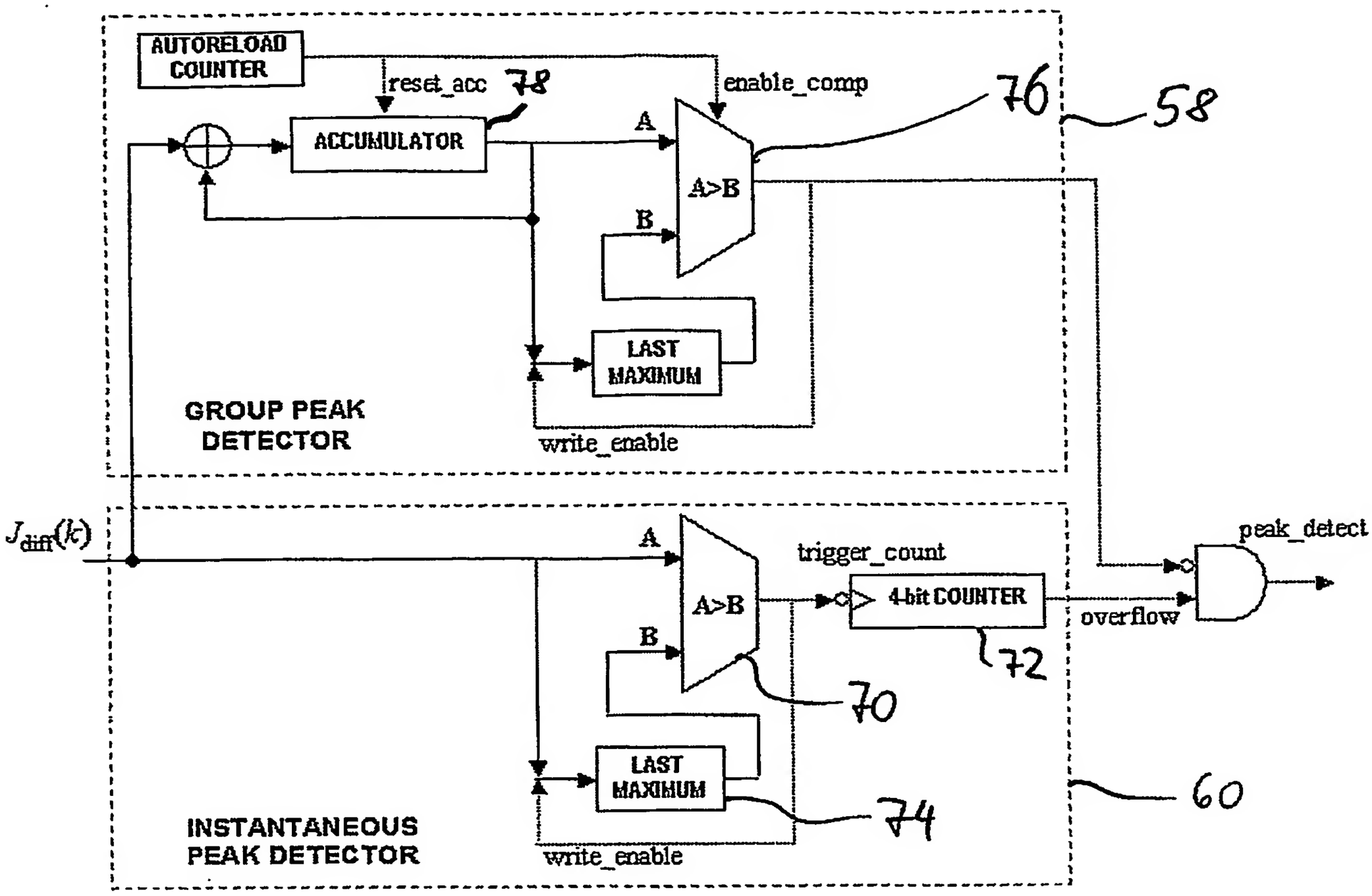

AUTORELOAD COUNTER
reset_acc
78
enable_comp
76
58
ACCUMULATOR
A
A>B
B
LAST MAXIMUM
GROUP PEAK DETECTOR
write_enable
$J_{diff}(k)$
A
A>B
B
trigger_count
4-bit COUNTER
overflow
peak_detect
72
70
LAST MAXIMUM
74
60
INSTANTANEOUS PEAK DETECTOR
write_enable

Fig. 8

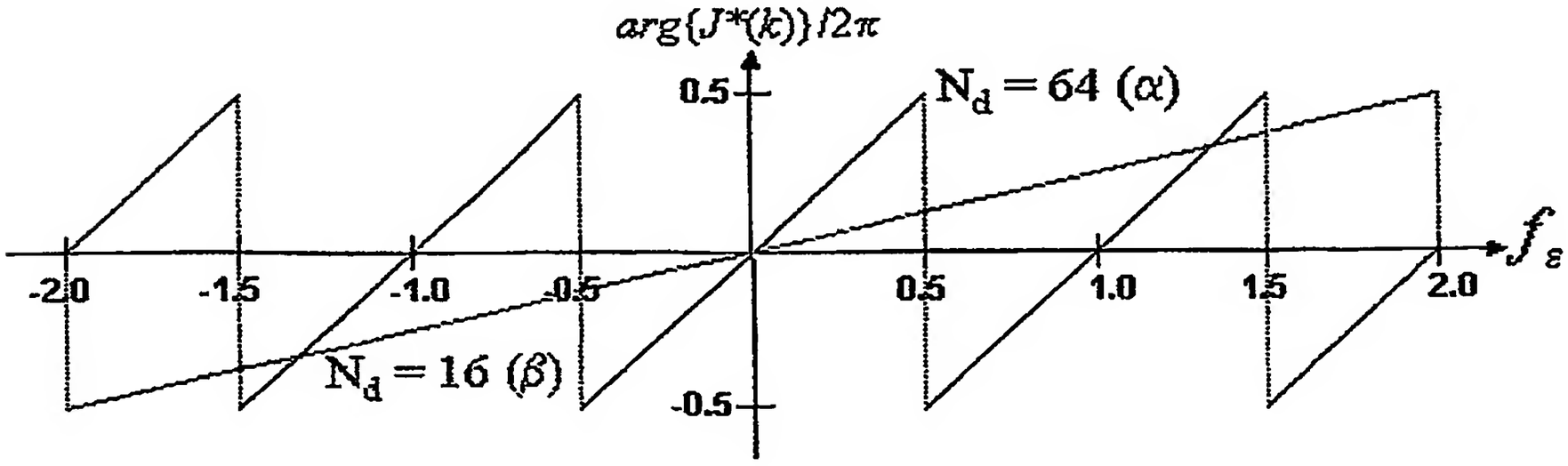

$arg\{J^*(k)\}/2\pi$
0.5
-0.5
$N_d = 64\ (\alpha)$
$N_d = 16\ (\beta)$
-2.0
-1.5
-1.0
-0.5
0.5
1.0
1.5
2.0
f_ε

Fig. 9

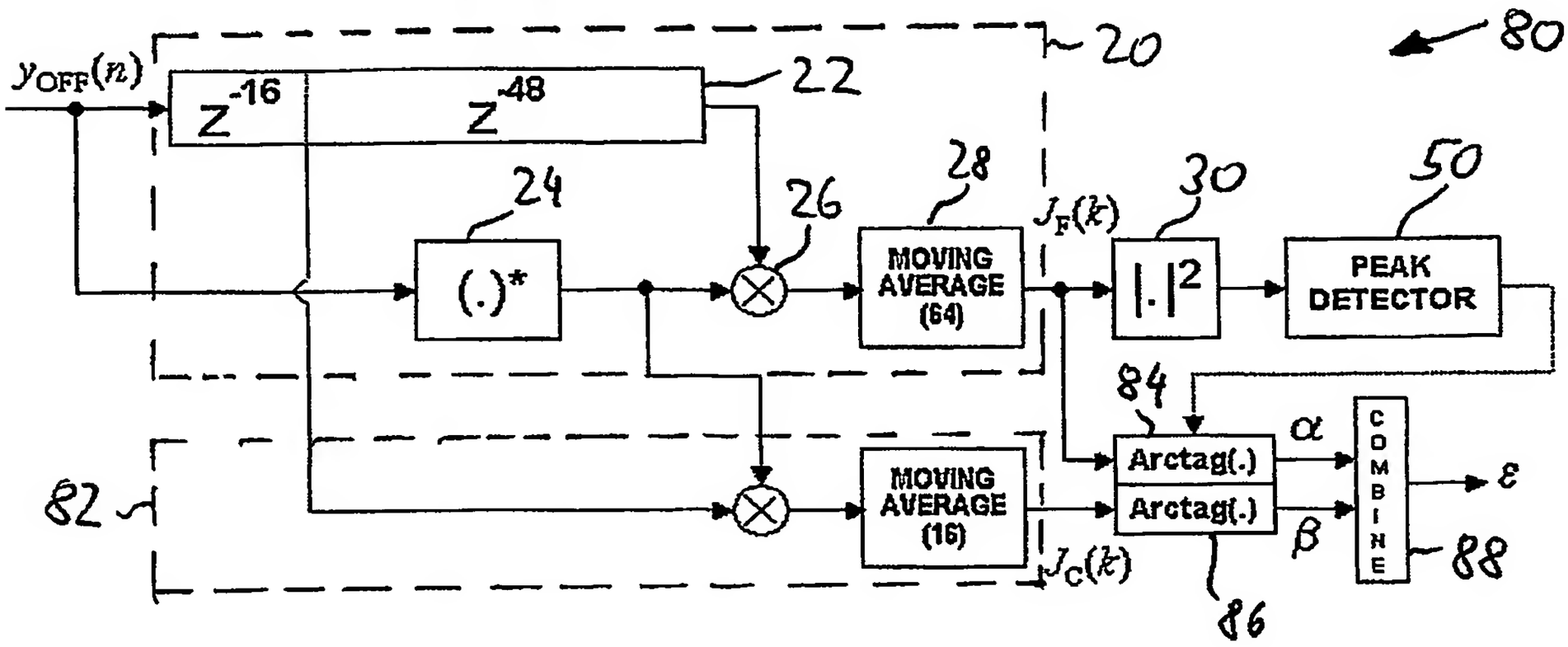


Fig. 10

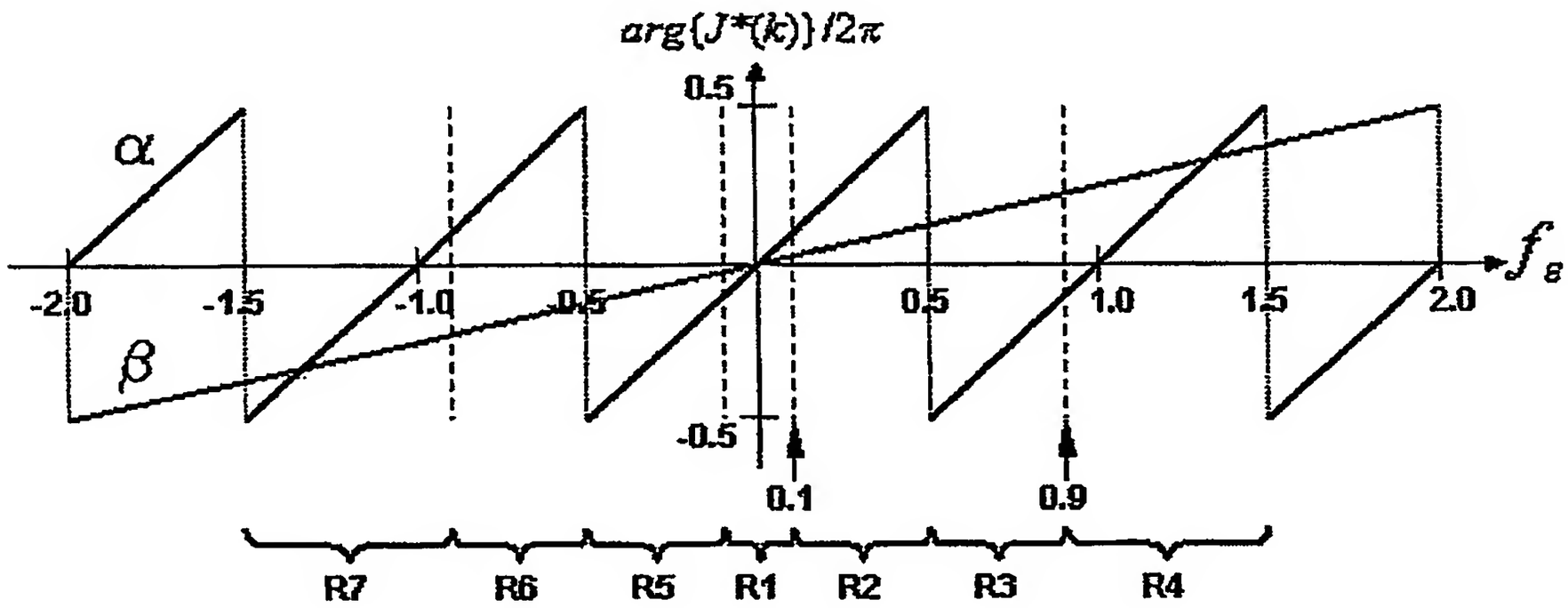


Fig. 11 a)

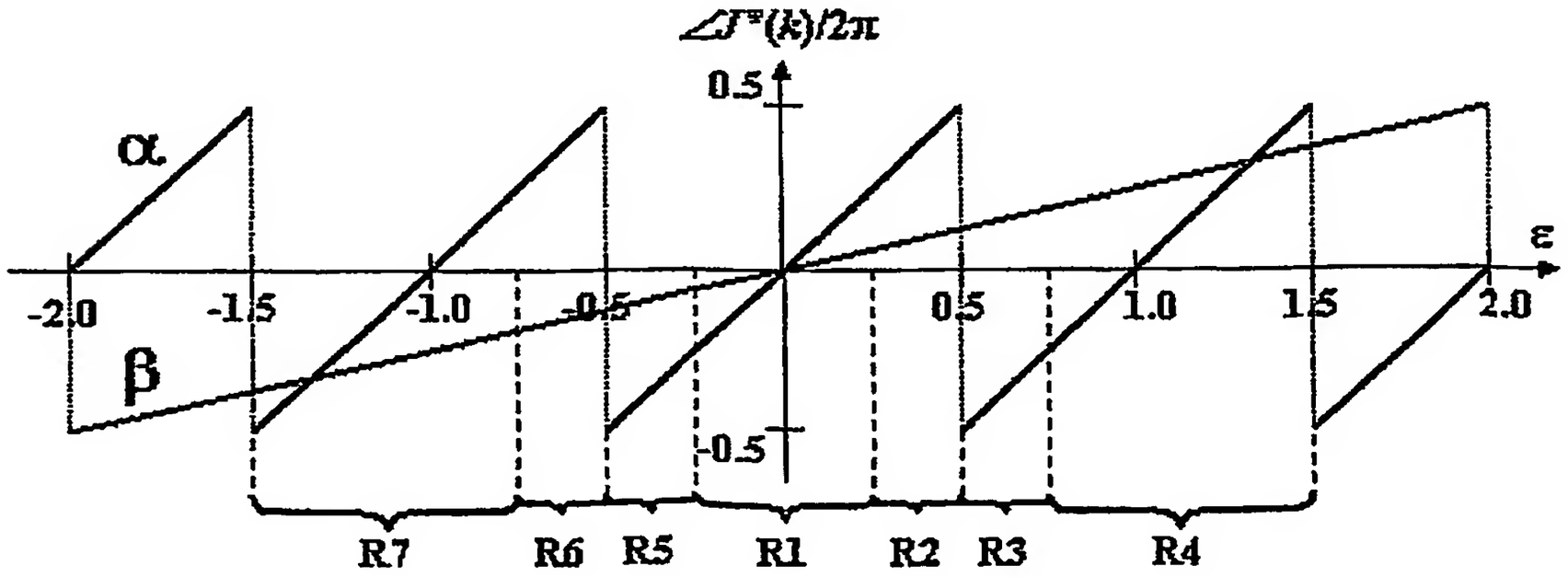


Fig. 11b)

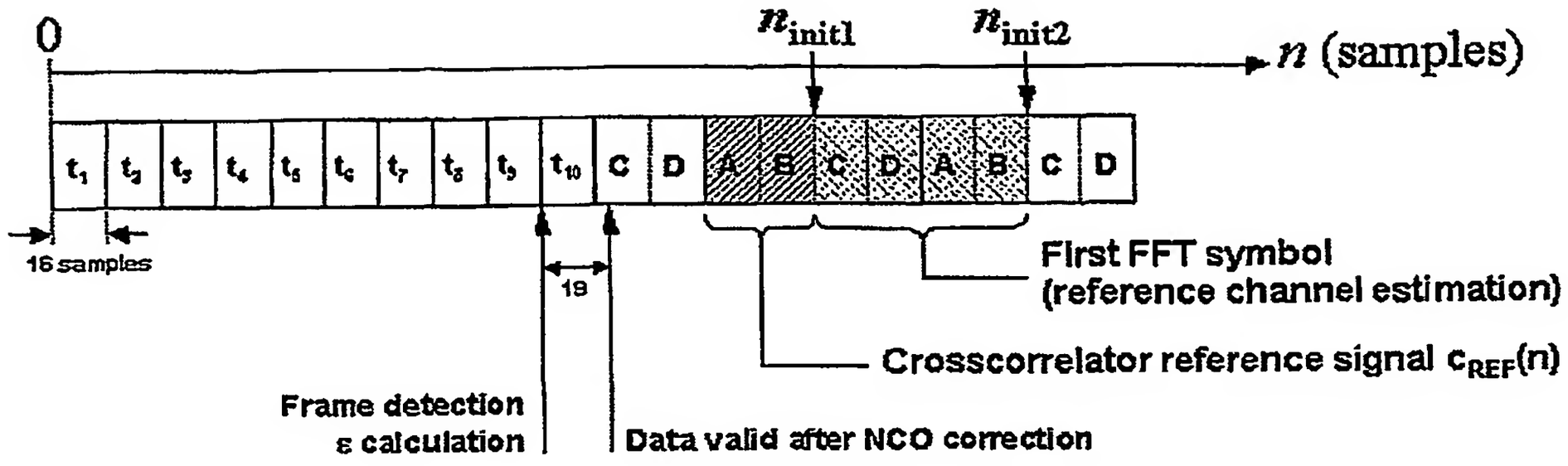

0
n_{init1}
n_{init2}
n (samples)
t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10} C D A B C D A B C D
16 samples
19
First FFT symbol
(reference channel estimation)
Crosscorrelator reference signal $c_{REF}(n)$
Frame detection
ε calculation
Data valid after NCO correction

Fig. 12

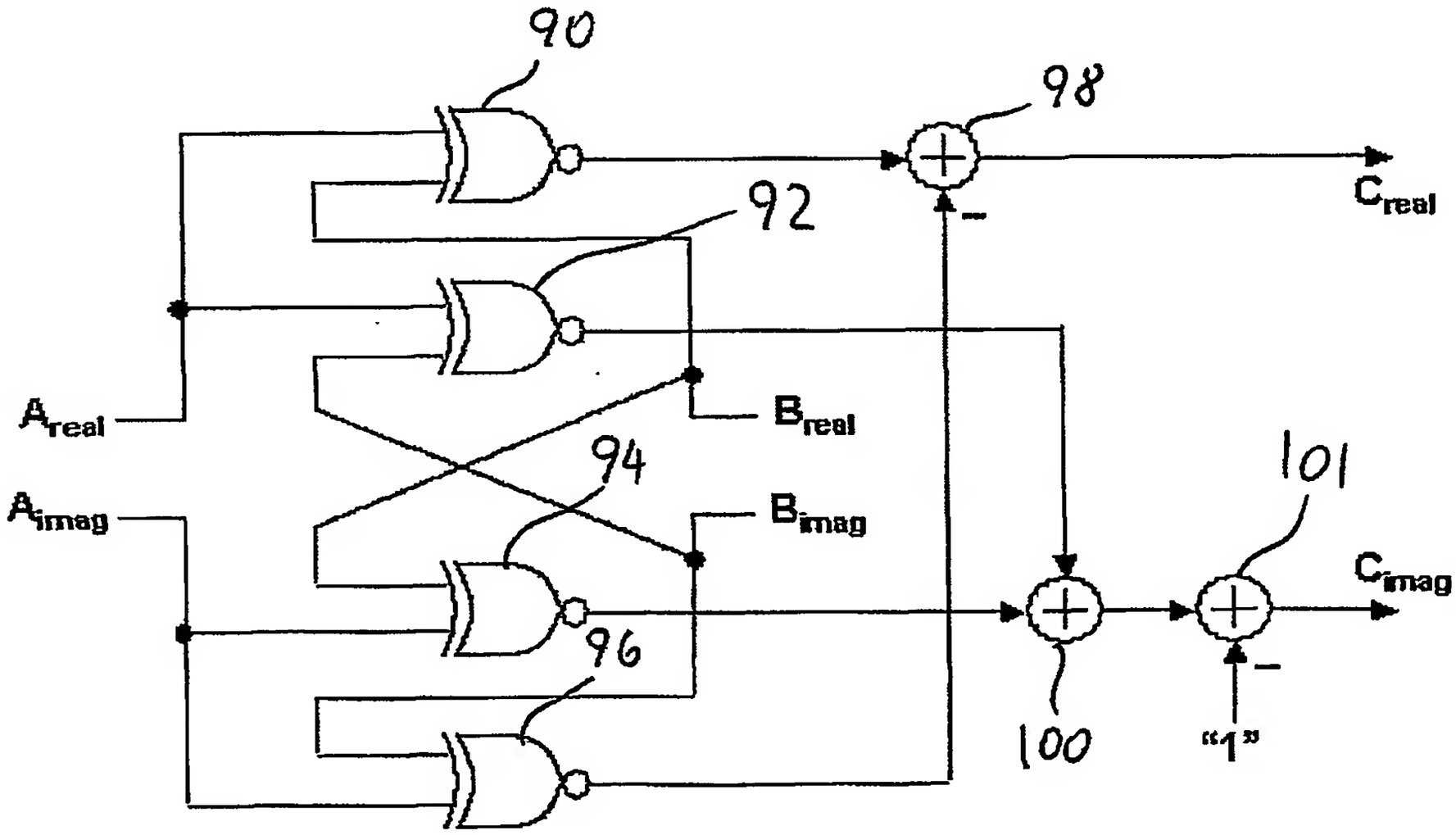

90
98
92
A_{real}
B_{real}
94
A_{imag}
B_{imag}
101
C_{real}
C_{imag}
96
100
"1"

Fig. 13

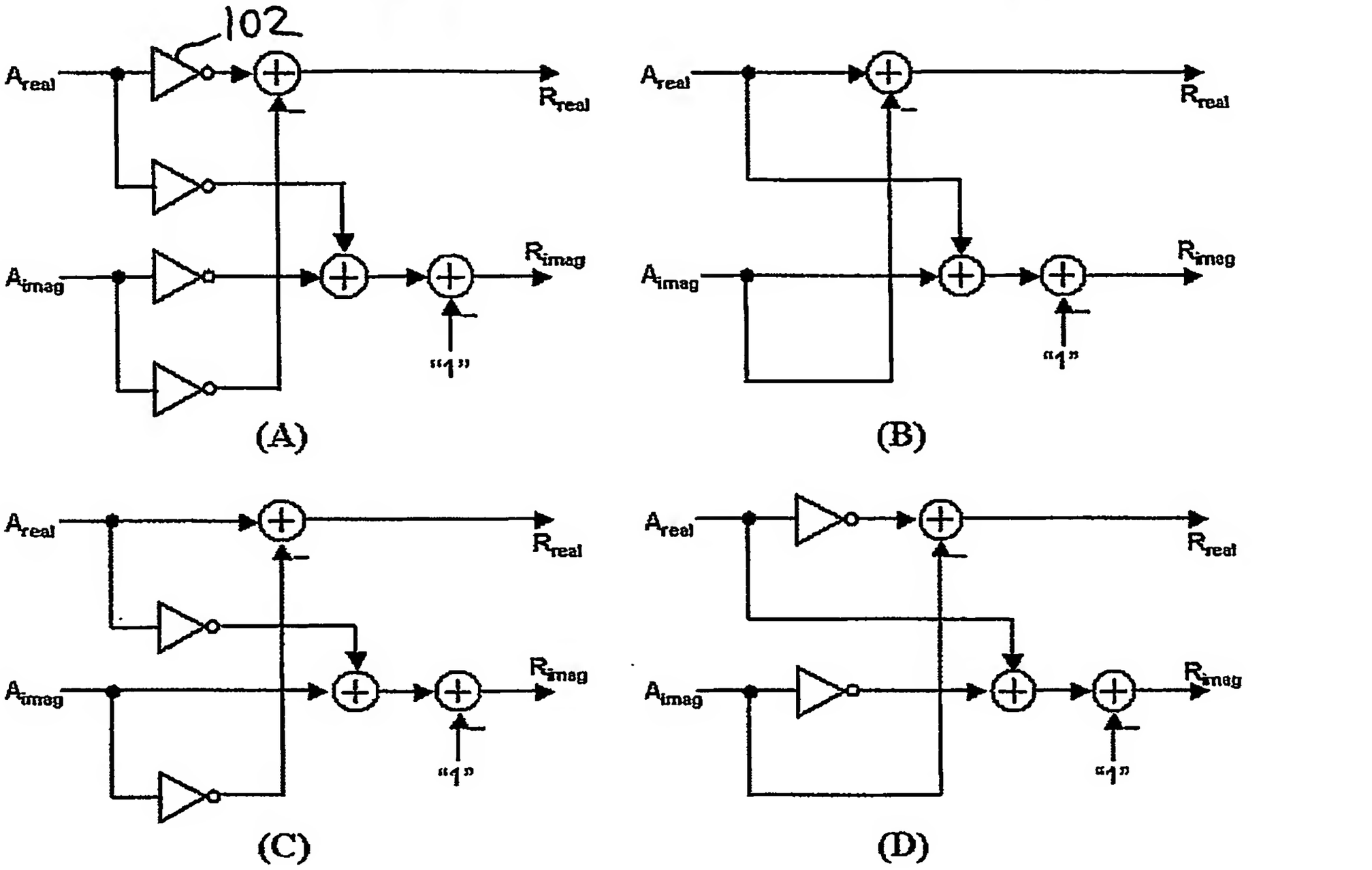

102
A_real
A_imag
R_real
R_imag
"1"
(A)
(B)
(C)
(D)

Fig. 14

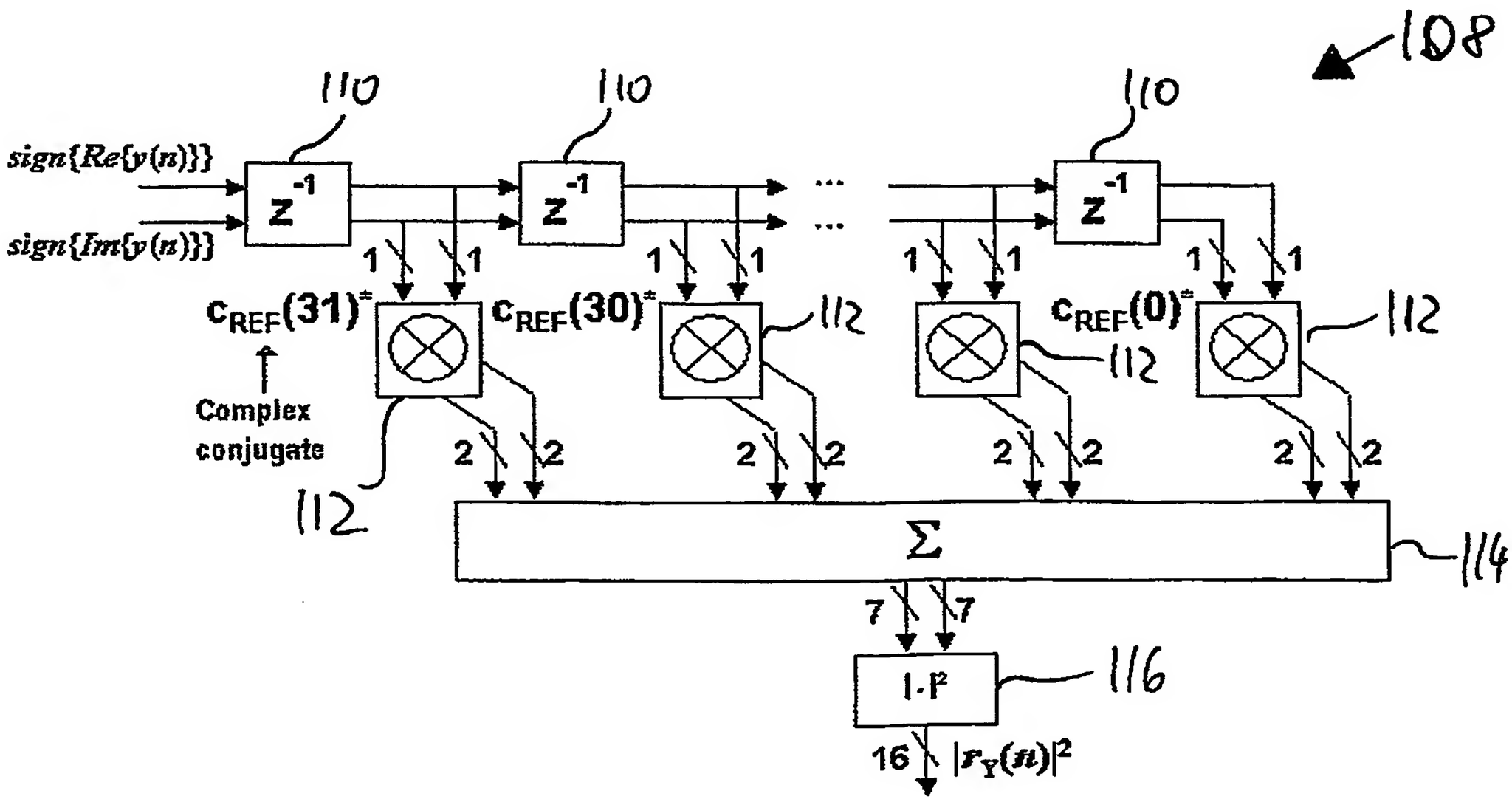

108
110
sign{Re{y(n)}}
sign{Im{y(n)}}
z^-1
1
c_REF(31)*
c_REF(30)*
c_REF(0)*
112
Complex conjugate
2
Σ
114
7
1·|²
116
16
|r_Y(n)|²

Fig. 15

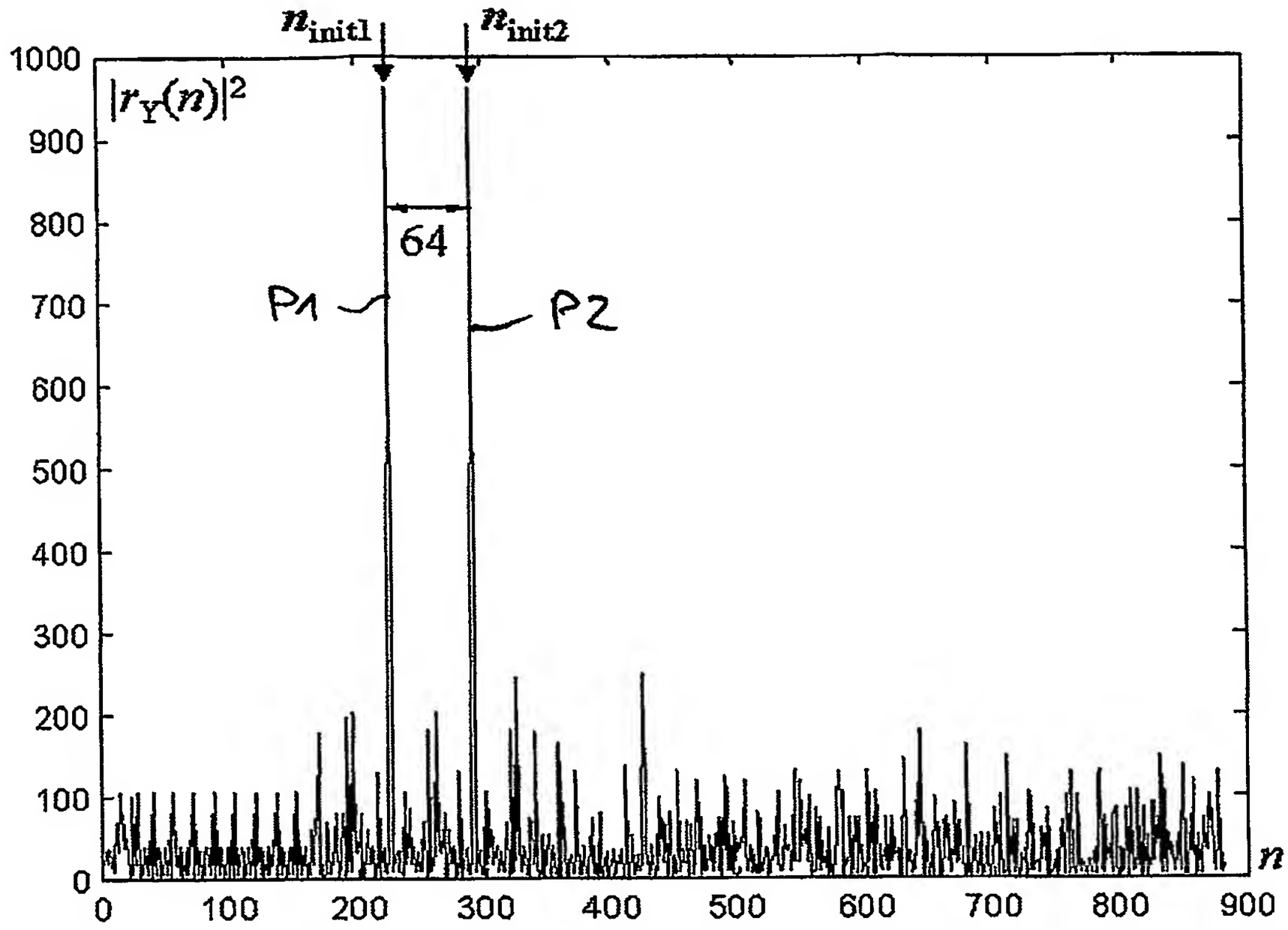

n_{init1}
n_{init2}
$|r_Y(n)|^2$
64
P1
P2
1000
900
800
700
600
500
400
300
200
100
0
0
100
200
300
400
500
600
700
800
900
n

Fig. 16

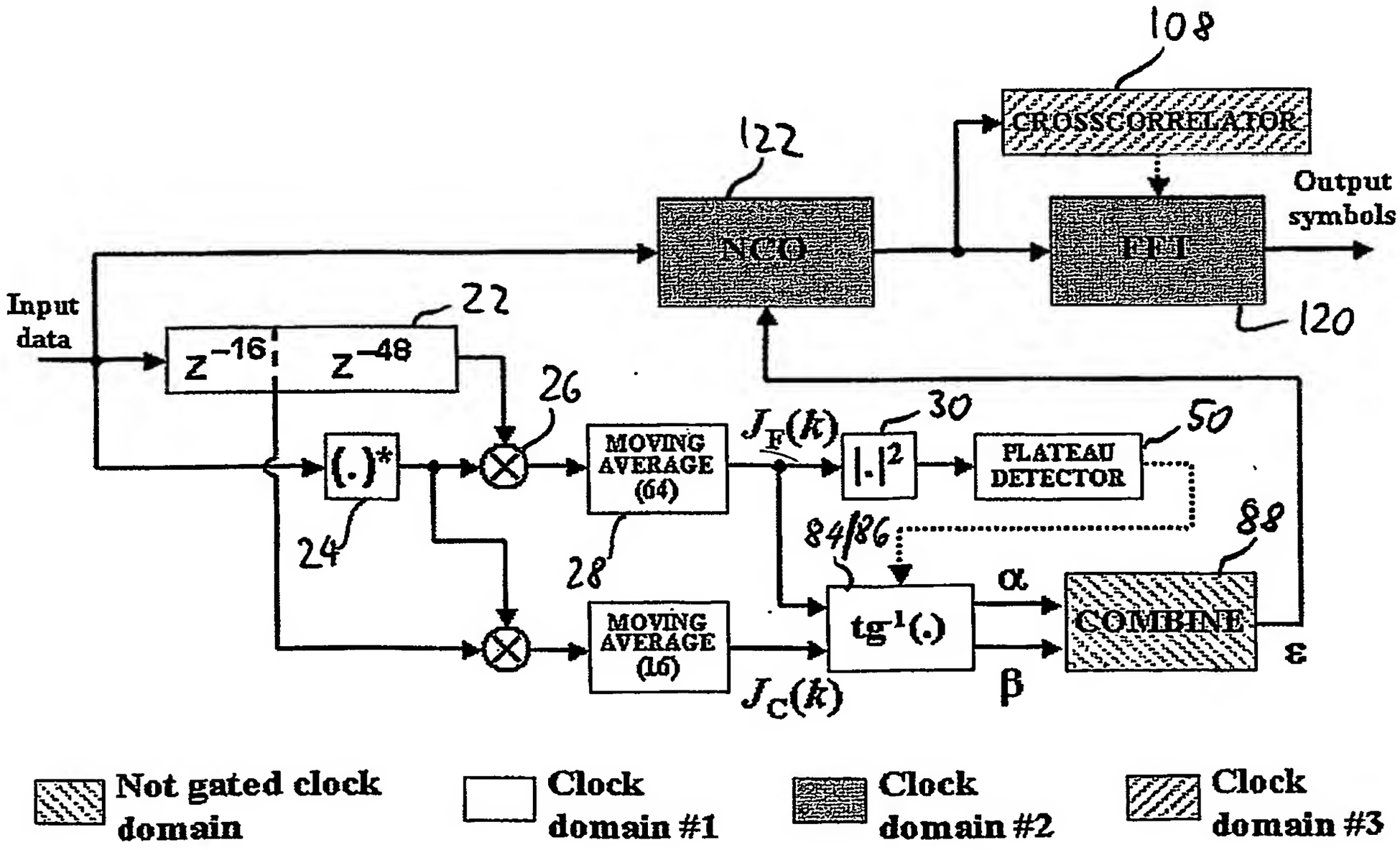

108
CROSSCORRELATOR
122
NCO
PLL
Output symbols
120
Input data
22
z^{-16}
z^{-48}
26
(.)*
24
MOVING AVERAGE (64)
28
$J_F(k)$
30
$|.|^2$
PLATEAU DETECTOR
50
84/86
88
MOVING AVERAGE (16)
$tg^{-1}(.)$
α
β
COMBINE
ε
$J_C(k)$
Not gated clock domain
Clock domain #1
Clock domain #2
Clock domain #3

Fig. 17

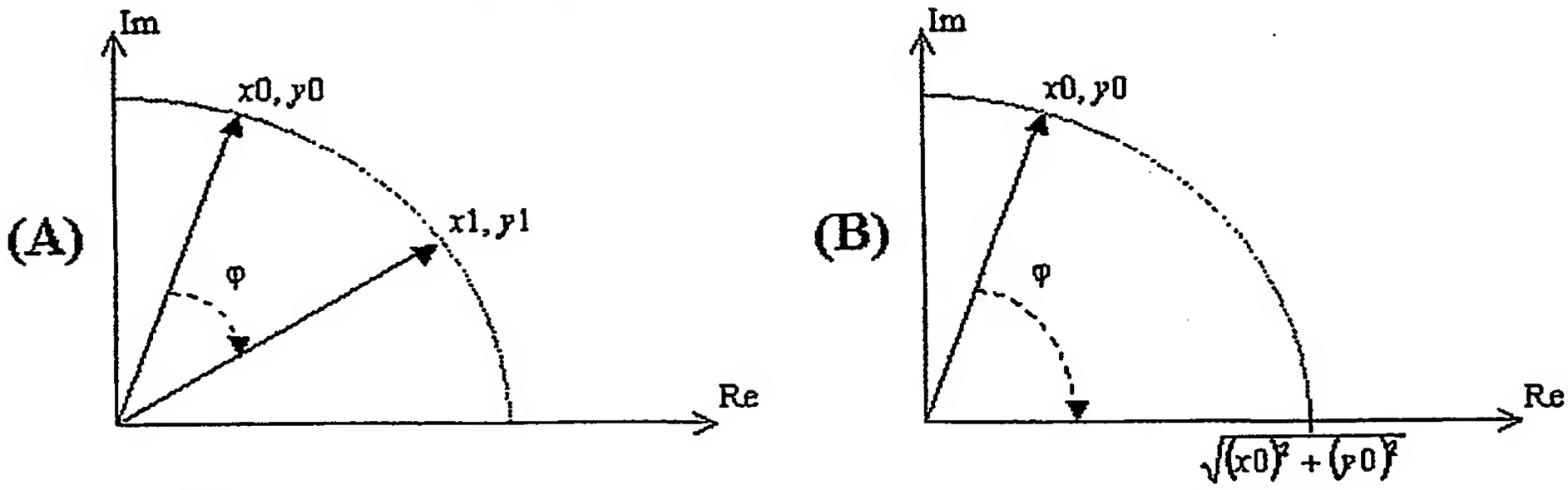

(A)
Im
x0, y0
x1, y1
φ
Re
CORDIC Inputs: x0, y0, φ
CORDIC Outputs: x1, y1
(B)
Im
x0, y0
φ
Re
$\sqrt{(x0)^2 + (y0)^2}$
CORDIC Inputs: x0, y0
CORDIC Outputs: φ, $\sqrt{(x0)^2 + (y0)^2}$

Fig. 18

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations JP, European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR)*

Published:
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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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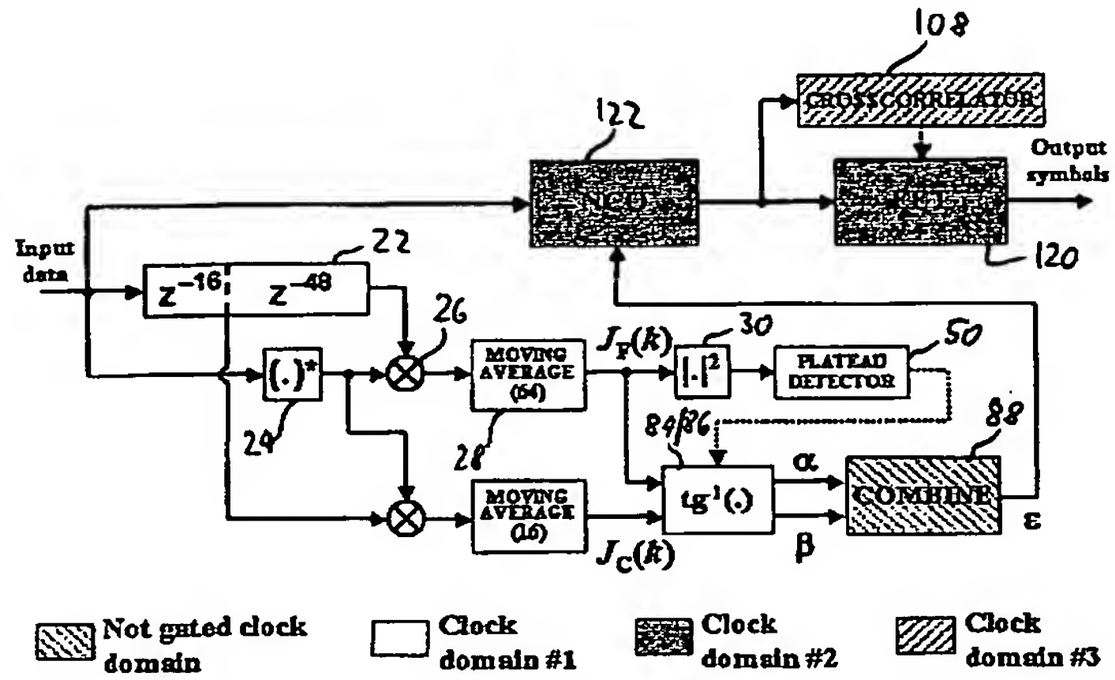
6 May 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND DEVICE FOR FRAME DETECTION AND SYNCHRONIZATION



(57) **Abstract:** The IEEE 802.11 a standard makes use of the Orthogonal Frequency Division Multiplex (OFDM) transmission scheme. The main feature of the OFDM is that the information stream is not transmitted into a single carrier, but is divided into several sub-carriers, each transmitting at a much lower rate. Furthermore, all these sub-carriers are orthogonal, i.e. they overlap their spectra but without causing mutual interference. In summary, there are the following inventions comprised in present application: the algorithm used for the frame detection, making use of a simplified differentiator to obtain an absolute maximum in the differentiated signal at that point where the first plateau in $J_F(k)$ starts (output of the autocorrelator with $N_d=64$); the design of the peak detector to obtain the position of the absolute maximum in the differentiated signal, dividing the problem into relative peak detection and falling edge detection; the use of a simplified XNOR-based crosscorrelator, and the simplifications therein based on the knowledge of the reference; the use of our particular solution for the CORDIC algorithm in the vectoring mode for arctangent calculation; the hardware structuring of the whole synchronizer, allowing a very simple control mechanism and the separation of this structure into different clock domains, each one being activated only to perform its operation and deactivated afterwards.

WO 2004/008706 A3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/[redacted]/07750

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L27/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 98/10545 A (BAHLENBERG GUNNAR ;HAAKANSSON SIWERT (SE); LJUNGGREN LIS MARIE (SE) 12 March 1998 (1998-03-12) page 41, line 25 - page 42, line 27; figures 11-14	1,4, 10-12, 14,16, 21,22, 25,27
A	EP 1 049 302 A (SONY INT EUROP GMBH) 2 November 2000 (2000-11-02) paragraph [0040] - paragraph [0042]	1-16,21, 22,25,27

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 December 2003	27.02.04

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Stolte, N

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

[redacted]

International application No
PCT/[redacted]3/07750

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	YUN CHIU, DEJAN MARCOVIC, HAIYUN TANG, NING ZHANG: "OFDM Receiver Design" [Online] , XP002263353 Retrieved from the Internet: <URL:http://bwrc.eecs.berkeley.edu/People/ Grad_Students/ dejan/ee225c/ofdm.pdf> [retrieved on 2003-11-26] Section 2.3 and 2.4 Section 4	1-16,21, 22,25,27
A	GRASS E ET AL: "ON THE SINGLE-CHIP IMPLEMENTATION OF A HIPERLAN/2 AND IEEE 802.11 A CAPABLE MODEM" IEEE PERSONAL COMMUNICATIONS, IEEE COMMUNICATIONS SOCIETY, US, vol. 8, no. 6, December 2001 (2001-12), pages 48-57, XP001076795 ISSN: 1070-9916 page 54, right-hand column - page 55, left-hand column	1-16,21, 22,25,27
P,X	KRSTIC M ET AL: "Optimized low-power synchronizer design for the IEEE 802.11a standard" 2003 IEEE INTERNATIONAL CONFERENCE ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING. PROCEEDINGS. (ICASSP). HONG KONG, APRIL 6 - 10, 2003, IEEE INTERNATIONAL CONFERENCE ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING (ICASSP), NEW YORK, NY: IEEE, US, vol. 1 OF 6, 6 April 2003 (2003-04-06), pages 333-336, XP010640949 ISBN: 0-7803-7663-3 the whole document	1-16,21, 22,25,27
P,X	A. TROYA, K. MAHARATNA, M. KRSTIC, E. GRASS, R. KRAEMER: "OFDM Synchronizer Implementation for an IEEE 802.11a Compliant Modem" PROCEEDINGS OF THE IASTED INTERNATIONAL CONFERENCE, WIRELESS AND OPTICAL COMMUNICATIONS JULY 17-19, 2002, 17 July 2002 (2002-07-17), - 19 July 2002 (2002-07-19) pages 152-157, XP009022041 Banff, Canada the whole document	1-16,21, 22,25,27

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP 03/07750

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-16, 21, 22, 25, 27

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-16, 21, 22, 25, 27

These claims are directed in general to different synchronization steps, and in particular to frame synchronization.

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2. claims: 17-20

These claims are in particular directed to frequency offset estimation.

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3. claims: 23, 24, 28, 29

These claims are in particular directed to symbol timing estimation.

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4. claim: 26

This claim is in particular directed to reference channel estimation.

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5. claim: 30

This claim is directed to power consumption reduction of the device.

INTERNATIONAL SEARCH REPORT

[redacted] on patent family members

Internati[redacted]blication No
PCT/E[redacted]03/07750

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9810545 A	12-03-1998	SE 506634 C2	26-01-1998
		AT 249118 T	15-09-2003
		DE 69724625 D1	09-10-2003
		EP 0923821 A1	23-06-1999
		NO 990767 A	30-04-1999
		SE 9603187 A	25-11-1997
		WO 9810545 A1	12-03-1998
EP 1049302 A	02-11-2000	EP 1049302 A1	02-11-2000
		CA 2305168 A1	23-10-2000
		CN 1272014 A	01-11-2000
		JP 2000341244 A	08-12-2000